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INSTRUCTION BOOK

MODEL 60-DC
CODED TIME SOURCE

PART OF

FLIGHT SERVICE AUTOMATION SYSTEM

CONTROLLED DOCUMENT

CONTRACT DTFA01-81-C-10039

CONTRACTOR

E-SYSTEMS, INC.
GARLAND DIVISION
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MADE FOR

U.S. DEPARTMENT OF TRANSPORTATION

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RECORD OF CHANGES

CHANGE TO BASIC	SUPPLEMENTS			OPTIONAL USE	CHANGE TO BASIC	SUPPLEMENTS			OPTIONAL USE

FAA Contract DTFA01-81-C-10039
Contractor: E-Systems, Inc., Garland Division
Subcontractor: Kinemetrics/True Time Instruments

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SECTION I

GENERAL INFORMATION

1-1 INTRODUCTION

1-2 This manual has been designed and written to provide the owner of the Model 60-DC WWVB Synchronized Clock with all the data and information needed to operate and utilize all its features.

1-3 The information included in this manual is as complete as possible and includes normal maintenance and adjustment data that may be required to facilitate field repair of the unit.

1-4 The Model 60-DC has been designed to receive the National Bureau of Standards radio station WWVB, transmitting on 60kHz, decode the time information and display time of year on a front panel display. Also available are outputs for supplying the time information to other equipment. The Synchronized Clock in its standard configuration provides a front panel display of days, hours, minutes, and seconds with five rear panel BNC connectors with IRIG B, 1Hz, 1 kHz, Precision 60 Hz, and Slow Code locked to the display. The electrically outputted time (and options if ordered), may be in either Universal Coordinated Time (UTC), more commonly referred to as Greenwich Mean Time (GMT), or in local time. This is done through the proper time zone offset selected by the rear panel thumbwheel switches. The Model 60-DC is shipped to display the time of year in the twenty-four hour format. By simply removing the cover and switching the position of the small switch on the microprocessor circuit board, the unit can be converted to display and output time in the more conventional twelve hour format.

1-5 This instrument has been designed to be completely automatic, only requiring antenna installation and connection of the unit to the power source. Once the instrument is turned on, the microprocessor will lock to the signal from WWVB, decode and display the time. From that point on, the unit will require no further attention and will provide time to an accuracy of $\pm$.5ms, continually updated by and phase locked to the National Bureau of Standards, In the event of loss of signal, the unit will continue operation on its internal crystal time base. If power should fail, upon restoration, the unit will again read the time signals and start displaying the time as transmitted by WWVB.

1-6 The Synchronized Clock is guaranteed to operate at any location within 1800 air miles of the transmitter in Boulder, Colorado. The unit can also be expected to operate properly at any location within the Continental United States and other areas over 1800 miles from the transmitter where WWVB's time code can be received. Our experience indicates that the receiver will operate satisfactorily down to signal strengths of 20μv/m, when there is not an otherwise overriding R.F. signal.

1-7 WARRANTY

TRUE TIME INSTRUMENTS warrants each instrument it manufactures to be free from defects in its material and workmanship for a period of two years from the date of delivery. Under this warranty any instrument which is returned to us (freight pre-paid) and is found by us to be defective in material or workmanship will be repaired or replaced (at our option) and returned at no charge to the customer.

Our obligation under this warranty is limited to servicing or adjustment of any instrument returned. Items not covered by this warranty are: fuses, batteries, and any illuminated parts or damage caused by accident or physical destruction of the instrument.

This warranty is expressly in lieu of all other obligations or liabilities on the part of TRUE TIME INSTRUMENTS. TRUE TIME INSTRUMENTS neither assumes nor authorized any other person to assume for them any other liability in connection with our sales.

This warranty is applicable in the United States and Canada only. For other areas, consult "KINEMETRICS,INC."

1-8 SPECIFICATIONS

RECEIVER FREQUENCY:	60kHz - National Bureau of Standards Station WWVB.
SENSITIVITY:	0.5μv.
BANDWIDTH:	Effective Signal Bandwidth, code recovery- no interference between successive code bits.
	Effective Noise Bandwidth, code recovery- less than ±2 Hz.
	Effective Signal Bandwidth, 1 Hz sync.-±1kHz.
	Effective Noise Bandwidth, 1 Hz sync.- ±2Hz.
TIMING ACCURACY:	1)±0.5ms. of N.B.S. transmitted time, excluding propagation delay. 2)The time difference between neighboring clocks is considerably improved over UTC timing accuracy. Consult the factory for specification and conditions.
TIME BASE STABILITY:	Better than 50μs when phase locked to WWVB. Other times crystal controlled to ±6 X 10^{-6}.
DISPLAY:	½" high planar discharge. Displays hours, minutes and seconds. Day-of-Year, optional.
DISPLAY ACCURACY:	-0 to +100ms. any time colons are not flashing.
NOMINAL TURN-ON TIME:	Five minutes from power on and signal reception with 90% confidence under average signal conditions.
OPERATING TEMP:	0° to 50° C.
REAR PANEL OUTPUTS:	
1Hz:	Rising edge on time, drives ten TTL loads or CMOS. High 10%, Low 90%. See Section 3-19.
1kHz:	Rising edge on time, drives two TTL loads or CMOS. High 10%, Low 90%. See Section 3-21.

REMOTE DISPLAY DRIVING (IRIG B): IRIG B Time Code is provided on a rear panel BNC connector. Standard IRIG B Time Code is an amplitude modulated 1kHz carrier. This output can also be easily field converted to TTL compatable D.C. level shift time code. See Section 3-23.

SLOW CODE: BNC output of 1 pulse per minute (1ppm), 1 pulse per hour (1pph), and 1 pulse per day (1ppd). The pulses go high on time and remain high for 2 seconds for minute mark, 4 seconds for hour mark and 6 seconds for day mark. Capable of sourcing 40 MA at 4.0 volts minimum, and pulled to ground by a 1k Ω resistor. See Section 3-30.

60 HZ: Provided on BNC connector as frequency source to drive a synchronous motor through a power amplifier. Capable of sourcing 100μa at 2.4V and sinking 1.6MA at .4V. (TTL Load). The output square wave has an unusual duty cycle. The 60 Hz is a 50% duty cycle over 50 ms (3 cycles).

Cycle #1	High 9ms, Low 8ms
Cycle #2	High 8ms, Low 9ms
Cycle #3	High 8ms, Low 8ms

See Section 3-35.

EXTERNAL OSCILLATOR (*OPT.*) Input level of less than 4V and greater than 2.4 volts (TTL) sine wave or square wave is required. Any frequency from 100 kHz to 10MHz in multiples of 100kHz is satisfactory. No unit adjustment is needed regardless of frequency. Used as clock timebase when not phase locked to WWVB. See Section 3-39.

IRIG H (*OPTION*): BNC output of standard IRIG H format TTL DC level shift supplied unless otherwise requested. If 1kHz amplitude modulated carrier requested, IRIG B will automatically be supplied in D.C. Level Shift format. See Section 3-44.

PARALLEL BCD TIME (*OPTION*): If ordered, Parallel BCD time of year is provided on rear panel 50 pin "D" connector. Days, hours, minutes, seconds and milliseconds are provided. Lines indicating worst-case time error of +1, +5, +50 and +500ms drives 2 standard "TTL" loads or "CMOS". See Section 3-48.

HOURS OFFSET:	Rear panel thumbwheel switch allows subtraction of "0" to "11" hours from transmitted UTC time. See Section 3-10.
12/24 HOUR OPERATION:	Dip Switch located inside unit allows use as 12 hour clock in place of 24 hour format as shipped. See Section 3-12.
SIZE:	1-3/4" x 17" x 10½" (4.4 x 43.2 x 26.7cm) behind panel. Mounts in standard 19" (48.9cm) EIA rack system, hardware included. 24" (60.9) hardware available.
WEIGHT:	7¼ lbs. (3.5kg) Ship Wt. 12 lbs. (5.4kg).
POWER:	95-135VAC, 60-400Hz, less than 25 volt amps. Others available on request.

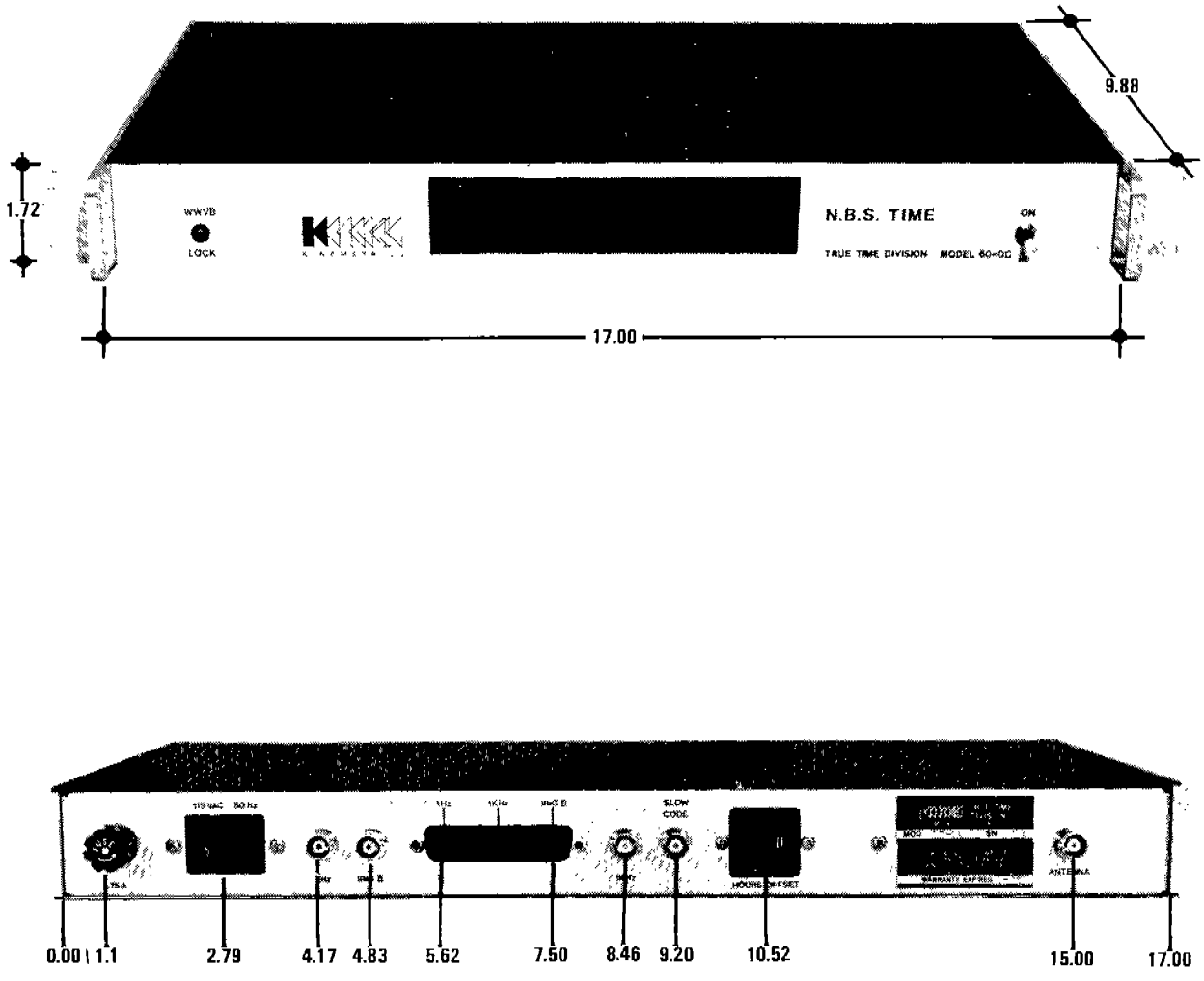


FIGURE 1-2 MODEL 60-DC DIMENSIONS

SECTION II

INSTALLATION

2-1 ANTENNA INSTALLATION

2-2 The Model 60-DC Synchronized Clock is shipped ready for operation and will require no adjustments. The first step in set-up and operation of the unit is to install the antenna. If the unit has been ordered with either the Model A-60FS or the Model A-60LW antenna manufactured by True Time Instrument Company, refer to the appropriate section of this manual for their installation instructions. Lead-in cable such as 50 ohm RG58/U is recommended. This coax is available through True Time Instrument Company in 50 and 100 foot lengths.

2-3 RACK MOUNTING

2-4 If it is desired to mount the Model 60-DC in a standard 19" rack system, the user can use the rack mounting ears provided with the unit. These ears may be attached to the side of the cabinet by removing the two 8-32 flat head screws on one side of the instrument and placing the screws through the counter-sunk hole in the bracket and re-installing the screw. The unit now may be mounted in a 1-3/4" opening in any EIA Standard 19" rack system.

2-5 INSTRUMENT START-UP

2-6 After the antenna installation is complete as described in Section 2-2 above, the lead-in coax should be connected to the rear panel BNC connector labeled "ANTENNA". Connect the power cord to the socket on the rear panel and plug the unit into an appropriate power source. The power switch on the front panel may now be turned on.

2-7 Initial indication of proper operation will be the colons, which will come on, blink off and then stay on. After 30 to 45 seconds the "WWVB LOCK" LED on the front panel should light, indicating reception of the signal from WWVB and within five minutes the display should light indicating the proper time. Detailed explanation of each feature of the Model 60-DC is more fully described in Section III of this manual.

2-8 One of the most often overlooked and yet most important factors in the installation and operation of the

Model-DC is proper installation of the antenna. Without a proper antenna installation, the signal from the transmitter will not be received and thus the unit cannot possibly function properly. In many cases "just to try it out", (when the A-60FS antenna is ordered) an attempt will be made to operate the unit with the antenna inside of a building. This, as often as not, results in inability to phase lock to the signal. In some cases phase lock may be obtained, but the low signal level in these cases will be too low for the unit to read the time code information. Thus, the display will not light or will require extremely long periods of time to read two time frames properly and to turn on the digital display. If it is desired to view the received WWVB signal on an oscilloscope, refer to Section 5-21.

SECTION III

OPERATION

3-1 INTRODUCTION

3-2 The Model 60-DC Synchronized Clock provides the user with a means of obtaining time traceable to the U.S. National Bureau of Standards with an accuracy of $\pm$.5ms. For stability the time base is phase-locked to the carrier of WWVB, which is transmitted to an accuracy of a few parts in 10^{-12}. The time-of-year information broadcast by WWVB is displayed in day-of-year, hours, minutes and seconds on the front panel. Also, available are outputs of this time information in the form of IRIG H, Parallel BCD, RS-232C compatable interface, or IEEE-488 compatability. The Model 60-DC has been specifically designed to minimize operator set-up and will provide many years of service without attention.

3-3 WWVB LOCK

3-4 Located on the left hand lower corner of the front panel is a LED labeled "WWVB LOCK". This green LED will light any time the unit is receiving sufficient signal from WWVB to allow the internal time base to phase lock to the carrier frequency of 60kHz. When the unit is initially turned on, if adequate signal is present, this LED will light within 30 to 45 seconds. If during the course of operation phase lock with the transmitter is lost for over 16 seconds this light will go out. If phase lock is lost for extended periods of time, due to the long time constant of the phase lock loop, it will take somewhat longer than 45 seconds to re-acquire phase lock when reception is regained.

3-5 Phase lock will be maintained continually in most areas and the only occasion for loss of lock will be short periods of time during the time when the day/night line is between the transmitter in Boulder, Colorado and the location of the receiver. This time is referred to as "diurnal" and can result in the signal level dropping to almost zero and returning to normal levels within a period of less than ½ hour. The second possible cause for loss of reception would be a transmitter failure. Although this is a very rare situation (during 1975 there were 11 outages totalling 168 minutes), it should be considered if reception cannot be obtained. In Section 3-8 to follow, a complete description of display indications of time accuracy, based on phase lock with the WWVB carrier, is explained.

3-6 DISPLAY

3-7 The front panel display of time is blanked when the unit is initially turned on, beacuse the correct time is not known. The time information braodcast by WWVB is a "slow code" and has a time frame of one minute. The time information is broadcast in the first 35 seconds of each minute. Requirements for the display to light are: 1) the unit must obtain phase lock with the carrier of WWVB and, 2) two consecutive minutes of time code must be read which agree as to the time. When these two criteria are met the display will light showing the correct time in days, hours, minutes, and seconds, Universal Coordinated Time (UTC) more commonly referred to as Greenwich Mean Time (GMT). Correction to local time, conversion to a 12-hour clock in place of the 24-hour time base as transmitted and correction for propagation delay are covered in the following sections.

3-8 The display has been designed to indicate to the user the accuracy of the time information being displayed and on the time output lines if ordered. After the display turns on it will indicate the worst case accumulated drift of the time information should phase lock with the transmitter be lost. When the unit has accumulated loss of lock for two hours since the last synchronization to $\pm$5ms., the colons will flash. The flashing colons indicate that the estimate of the worst-case error of the display and outputted time is $\pm$50ms. of N.B.S. time. When the unit has been in operation for a cumulative twenty-hours without phase lock since the last synchronization, the complete display will flash. This flashing is certain to attract the operators attention and indicates that the time as displayed and outputted may have a worst case error of more than $\pm$500ms. (½ second)

3-9 Display or colon flashing will stop when the signal from WWVB is regained, phase locked to and the time code is read. Under normal operation this will occur without operator attention. It is very unlikely that either of these conditions will occur within reasonable distances from the transmitter. Due to the nature of the unit to phase lock to the carrier frequency down to very low signal levels, persistant flashing of the colons or display may be an indication of poor reception due to local interference or antenna location and/or installation. Refer to Section V "Maintenance and Troubleshooting" for additional information on this subject.

3-10 HOURS OFFSET

3-11 Located on the rear panel is a thumbwheel switch

labeled "HOURS OFFSET". This switch is set for "0" at the factory which means the displayed time will be Universal Coordinated Time as broadcast. To change the hours on the display to read local time, set the switch to the number of hours your location is offset from Greenwich, England. For example, if you are located in the Eastern Time Zone and desire to display Local Standard Time, the switch should be set for "5", or for Daylight Savings Time,set for "4". If, in this case, the display was indicating 1800 UTC, the clock would subtract 5 hours and display 1300 hours for Local Standard Time. If the unit has been ordered with electrically outputted time(Parallel BCD, RS-232, IEEE-488), these outputs will agree with the display. Additional information on these outputs is included in the following sections.

3-12 12/24-HOUR CLOCK OPERATION-

3-13 The Model 60-DC is shipped from the factory for operation on the 24-hour clock system as broadcast by the National Bureau of Standards. If it is desired to convert the clock to a 12-hour clock display, a small internal switch can be turned.

3-14 To convert a clock to the 12-hour format refer to Figure 3-1. Remove the four screws retaining the lid and slide the swtich indicated in the photograph to the 12-hour position. Replace the cover and reinstall the screws.

3-15 PROPAGATION DELAY

3-16 This feature is included with the Model 60-DC to allow the microprocessor to compensate for the delay in the displayed and outputted time and timing marks due to the time required for the signal to travel to the receiver from the transmitter.

3-17 This feature consists of two switches on the Digital Board Assembly. To adjust these switches, first remove the four screws which hold the top cover in place, remove the lid and set it aside. Refer to Figure 3-1 for identification of the "Prop. Delay Switches". The two switches can be combined to provide for a total of 99 ms, propagation delay for the unit. The switch toward the rear panel provides 0 to 9 ms. and the switch toward the front adds to this in steps of ten from 0 to 90 ms. Therefore, if it is desired to compensate for 19 ms. propagation delay, the front switch would be turned to 1 (for 10 ms) and the rear switch to 9 (for 9 ms).

3-18 To calculate the delay in the signal to your location, first determine the number of air line miles from the transmitter location (Ft. Collins, Colorado) to the receivers location and divide that number by 186. The resulting number will be the number of milliseconds delay in the signal from the transmitting antenna to your antenna. For example, if your location is 1350 miles air miles) from the transmitter the signal will require:

$$\frac{1350 \text{ miles}}{186 \text{ miles/millisecond}} = 7.26\text{ms}.$$

Rounding off this answer gives 7 milliseconds delay. Therefore, the switch should be set for "7". If it is desired to use the time data to the ±0.5ms. accuracy of the unit, the .26 millisceonds rounded off here should be used in further calculations involving the time data. After the switch has been set, replace the lid and screws thus preventing accidental readjustment of this setting by others.

3-19 1 HZ

3-20 The 1 Hz is provided as a rear panel BNC connector and can be used for a wide variety of timing functions. This output is a pulse going high as the second remains high for 100 milliseconds and going low for the remaining 900 milliseconds. This output is driven from a 2N3904 (Q3) on the microprocessor board (Assy. 86-42, see Section VI). The collector of Q3 is pulled up to +5VDC with a 3.3KΩ resistor. This output is taken off of pin #3 of assembly 86-42 and capable of driving 10 TTL loads.

3-21 1 KHZ

3-22 The 1kHz rear panel output is similar in form to the 1Hz above. It is a square wave going high on time, remaining high for 100 microseconds and low the remaining 900 microseconds. This output is driven by assembly 86-41 (See Section VI). This is then fed to assembly 86-42 in interconnecting wire(s) and to the rear panel from 86-42 pin number 17.

3-23 IRIG B (REMOTE DISPLAY DRIVING OUTPUT)

3-24 The primary purpose of the IRIG B time code output is to drive slave displays manufactured by True Time Instruments. This output consists of the standard IRIG B time code. Refer to Section XII for a full description of this code.

3-25 When using this code for other than driving the

True Time Model RD-B, it should be noted that four "Control Functions" are used. These control functions encode estimated time accuracy as fully described in Section XII.

3-26 This output is supplied on a rear panel BNC connector. When shipped, this output is in a 1kHz carrier amplitude modulated format but can be field converted to D.C. level shift code format. In addition to driving remote displays, this output can be used to synchronize commercially available Time Code Generators or direct recording on magnetic tape.

3-27 The modulated 1 kHz format is a sine wave driven by op amp U22(LM324) in series with 100Ω (R106). The high level of the code is 5 volts peak to peak ±.5v; the low level is 2 volts peak to peak ±.2v. This output is fed through S1 (the "AM" modulation switch) to the 86-42 board via pin number "P" and to the rear panel from terminal number 18.

3-28 If it is desired to convert the IRIG B time code from the amplitude modulated form as shipped to a level shift output, it is necessary to remove the lid and turn the switch labeled "AM" off and turn the switch labeled "TTL" on. See Figure 3-1.

3-29 The "TTL" level shifted IRIG code is driven by transistor Q3(3904) and is capable of driving 10 standard TTL inputs. The level shifted signal is fed through S2 ("TTL" modulation switch) to the 86-42 board via pin number "P" and to the rear panel from terminal number 18. Note that S1 and S1 should not be closed simultaniously.

3-30 SLOW CODE

3-31 The "Slow Code" output from the Model 60-DC has been provided primarily for the purpose of providing timing marks on drum recorders such as the Kinemetrics Inc. Model VR-1. This output is a single line which goes high once per minute. On minute marks the output remains high for two seconds, on hour marks the line is held high for 4 seconds and for the day mark, a six second high is provided.

3-32 This output is driven by Q1 on assembly 86-42. This is a MPS3702 transistor and will source 40 ma. at 4.0 VDC. This drive is provided from pin #2 on the assembly 86-42 through a wire to the rear panel BNC.

3-33 A second format of this slow code is provided and can be easily field converted. If the wire from pin #2 of

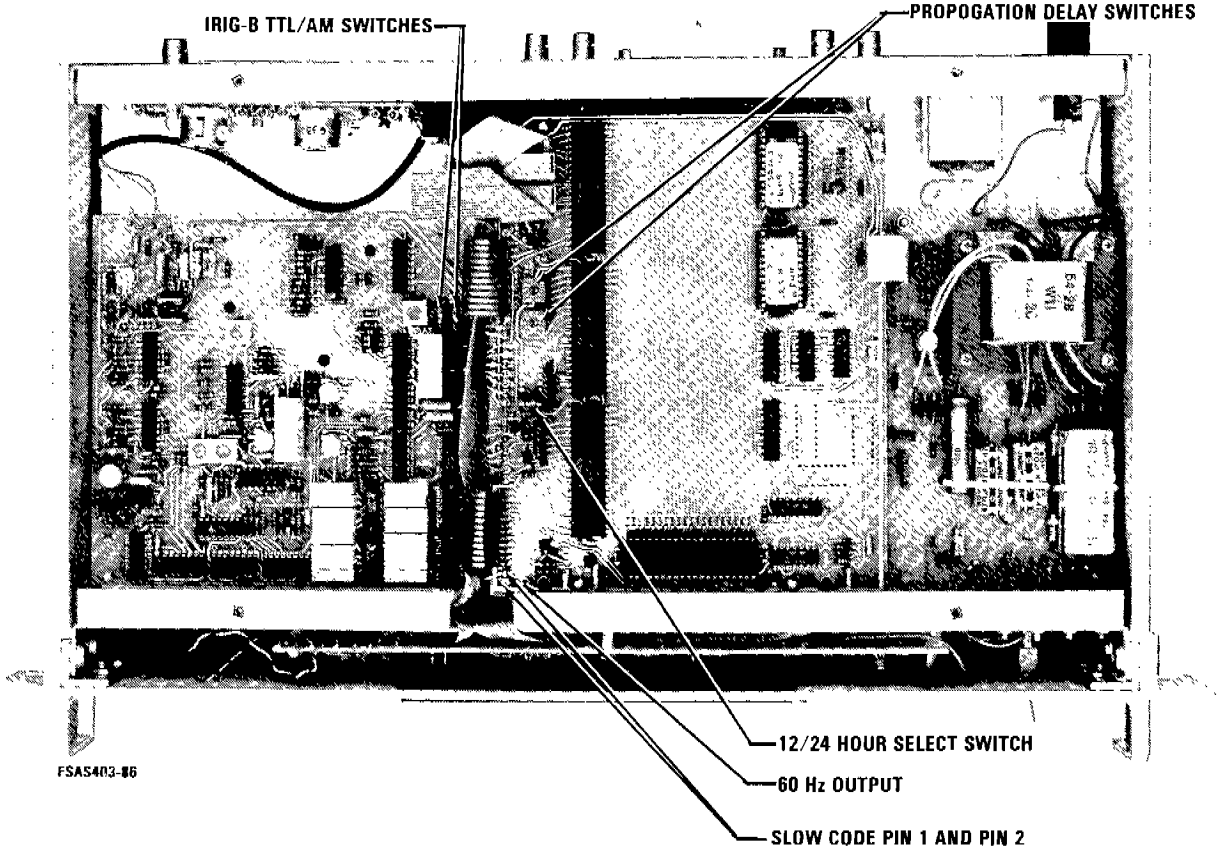


FIGURE 3-1 PARTS LOCATION - MODEL 60-DC

assembly 86-42 is connected to pin #1 on the assembly, the complement of pin #2 described above is provided. (See Figure 3-1). Pin #1 output is driven by Q2 (2N3904) with approximately 6KΩ pull up to 5VDC. This will drive 2 TTL loads. When wired in this manner, the output on the rear panel BNC will be normally high. On the minute it will go low 2 seconds, 4 seconds on the hour and 6 seconds for a day indicator.

3-34 NOTE: If "External Oscillator" option is ordered in conjunction with Parallel BCD, RS-232 or IEEE-488 output options, the "Slow Code" output is not on a rear panel connector but the user is free to lift the lid and obtain this output from pin #1 or #2 of assembly 86-42 for use.

3-35 60 HZ

3-36 The precision 60 Hz output on the rear panel BNC, like the Slow Code, has been provided primarily for the purpose of supplying a known 60 Hz signal to drive synchronous motors. This output, when supplied through a power amplifier such as the Kinemetrics Model PA-1, will provide a constant 60 Hz signal for driving drum recorders independent of local power line variations.

3-37 A quasi-square wave is provided for this purpose with transitions on exact milliseconds. The half cycle periods are 8ms, 8ms, 9ms, 8ms, 8ms and 9ms, etc., then repeating the pattern. This provides exactly a 60 Hz square wave after the average of three cycles.

3-38 Driven by U_{11} on assembly 86-42 (74LS00) this output is capable of driving 5 TTL loads. The output is from the front edge of assembly 86-42 from a bifurcated terminal labeled "60 Hz", through a wire to the rear panel connector.

3-39 EXTERNAL OSCILLATOR *(Special Order Option)*

3-40 If optionally ordered, this rear panel input provides for a local lab standard type of oscillator to be utilized as a clock time base during periods when phase lock with WWVB is lost.

3-41 The input frequency for this option may be anywhere between 100kHz and 10MHz in increments of 100kHz. The signal can be a sine wave or square wave with the low level less than 4V and the peak greater than 2.4 (TTL). This input is presented from the rear panel BNC through a coax to the input of U1 (74LS90), which has a 10KΩ pull up

to +5VDC. This input therefore is one TTL load.

3-42 Operationally, anytime the Model 60-DC is unable to phase lock to the 60kHz carrier of WWVB, the clock time base will utilize the provided input in the "External Oscillator" BNC connector. If frequency is not provided on this BNC, the 60-DC will continue to operate on its own internal crystal.

3-43 When the situation arises that lock to WWVB is lost, even if a cesium oscillator is used for the external oscillator, the indications of time drift continue. Therefore, the colons on the display and whole display will blank and flash in the usual manner to indicate loss of WWVB reception even in case of a "perfect" external time base. The output time error message in IRIG B, Parallel BCD, RS-232 and IEEE-488 also function to indicate loss of accuracy.

3-44 IRIG H *(Special Order Option)*

3-45 When ordered, IRIG H is provided on a rear panel BNC. If this is ordered in conjunction with Parallel BCD or RS-232 or IEEE-488, the 1Hz described in Section 3-19 is deleted in facor of this output. The 1Hz is available on assembly 86-42 as described but is not on a rear panel connector. The user can easily open the lid and obtain this 1Hz if desired.

3-46 The format of the IRIG H time code is covered in Section XII.

3-47 As shipped from the factory, the IRIG H Code is in D.C. Level Shift format. This output is provided through a 2N3904 (on Assembly 86-42) with a 3.3KΩ pull up to +5VDC. On request, this output can be supplied as a 1kHz amplitude modulated carrier. In this case, the IRIG B will be supplied as DC level shift.(See Section 3-23) The 1kHz generations and modulation system, originally used for the IRIG B, will then be used for the IRIG H, providing a 1kHz carrier amplitude modulated in IRIG H format as described in Section 3-23.

3-48 PARALLEL BCD TIME OUTPUT *(Special Order Option)*

3-49 The Parallel BCD Time Output option is designed to synchronize other equipment at the time provided by the National Bureau of Standards. This output consists of 42 lines of BCD data from 100's of days to units of milliseconds as shown in Figure 3-2. Also, included with this option are four lines to indicate the worst case error on the time outputted. One line indicates error of more than

±500ms, ±50ms, ±5ms and one indicated ±1ms. A 1Hz and 1kHz are available on the output connector which can be used to indicate to the user when the BCD time data on the lines are changing states. If this option is included, a 50 pin "D" connector has been installed on the rear panel.

3-50 All of the 42 BCD lines are driven by #CD4050B's and are capable of driving two TTL loads or multiple CMOS loads. These lines are high to indicate a one in that position in the BCD code. For further information regarding the output of these lines and their capabilities, refer to Section VI.

3-51 The pin of each output is shown in Figure 3-2 on the following page.

3-52 During normal operation, after start-up and synchronization with the WWVB, the four time quality lines will be in a low state. When phase lock with the transmitter is lost, the Model 60-DC will provide the user with a worst-case estimate of the accumulated clock drift based on the VCXO drift rate. This estimate is provided by each of the four lines changing to the high state in turn as the clock time base drifts from synchronization with N.B.S. When the time could be worse than ±1.0ms the output on pin #50 will go high, at ±5.0ms. Pin #14 will go high and on through pin #17 for worse than ±0.5 second accuracy. Each of these lines is driven by a RCA #CD4050 and is capable of driving two TTL loads or multiple CMOS loads. It will be noted that when the +50ms line goes high, the colons on the display will flash and when the ±500ms line goes high, the complete display will flash.

3-53 When phase lock is regained, the lines will again go low as the unit re-corrects to the proper time. On initial turn-on of the instrument or after a power failure, the +500ms line will remain in the high state until the display is turned on, thus indicating that the time on the parallel output lines is not correct to the accuracy indicated by the other lines, regardless of their state. This line can therefore be used as a read-inhibit line since the data should not be read when this line is in the high state. Refer to the 1 Hz and 1 kHz description below for additional parameters on reading the time of the Parallel Output option.

3-54 The 1 Hz output line on Pin #16 is driven by a #CD4050B and is capable of driving two TTL loads or multiple CMOS loads. This line goes to the high state on time and remains high for 900ms. At any time the 1 Hz line is high, the data on the parallel output lines from the seconds level up is not changing states and is available for reading.

PIN #	OUTPUT DATA	PIN #	OUTPUT DATA	PIN #	OUTPUT DATA
1	GROUND	18	2's of 10's of hrs.	34	8's of seconds
2	IRIG B Time Code	19	1's of 10's of hrs.	35	4's of seconds
3	2's of 100's of days	20	8's of hrs.	36	2's of seconds
4	1's of 100's of days	21	4's of hrs.	37	1's of seconds
5	8's of 10's of days	22	2's of hrs.	38	8's of 100's M-sec.
6	4's of 10's of days	23	1's of hrs.	39	4's of 100's M-sec.
7	2's of 10's of days	24	4's of 20's of mins.	40	2's of 100's M-sec.
8	1's of 10's of days	25	2's of 10's of mins.	41	1's of 100's M-sec.
9	1 kHz	26	1's of 10's of mins.	42	8's of 10's of M-sec.
10	8's of units of days	27	8's of minutes	43	4's of 10's of M-sec.
11	4's of units of days	28	4's of minutes	44	2's of 10's of M-sec.
12	2's of units of days	29	2's of minutes	45	1's of 10's of M-sec.
13	1's of units of days	30	1's of minutes	46	8's of units of M-sec.
14	$\pm$5ms. (See Note #2)	31	4's of 10's of sec.	47	4's of units of M-sec.
15	$\pm$50ms. (See Note #2)	32	2's of 10's of sec.	48	2's of units of M-sec.
16	1 Hz	33	1's of 10's of sec.	49	1's of units of M-sec.
17	$\pm$500ms. (See Note #2)			50	$\pm$1.0ms. (See Note #2)

NOTES:

1) Mating Connector TRW #DD-50P or equivalent.

2) Time accuracy lines in high state indicates time accuracy worse than level specified.

FIGURE 3-2 PIN OUT CONFIGURATION - PARALLEL BCD TIME DATA - MODEL 60-DC

3-55 If it is desired to read the milliseconds lines as well as the seconds through days, the 1 kHz line should be utilized as an indicator that the lines are not changing states. The 800's of milliseconds down to 1's of milliseconds are driven by synchronous counters and may be changing states during the first ½ microsecond of any millisecond.

3-56 The 1kHz line is driven by a #CD4049B and is capable of driving two TTL loads or multiple CMOS loads. The 1 kHz output can provide information to the user in two formats. The first format is as shipped from the factory. The second output format can be converted to in the field by two simple internal modifications.

3-57 As supplied from the factory, the 1kHz output on pin #9 of the "D" connector goes high on the millisecond for 500 microseconds and then goes low for the remaining 500 microseconds. Since the state of the Parallel Output Time data may be changing state during the first ½ microsecond of any millisecond, the transition from the low to the high state has been delayed to allow the milliseconds counter to stabilize. The rising edge of the 1kHz signal may be used as a Data Strobe. If, rather than one point in time, a time period of when it is "OK" to read is desired, the time period starting at the rise in level of the 1kHz line and continuing for the next 500 microseconds can be used. This 1kHz line should be used in conjunction with the +500ms line as described above to determine if the time data is correct and readable.

3-58 The second format for the 1kHz output line will provide an output which will go to the high state approximately 3.0 microseconds before the millisecond and low 2 microseconds later. This line will not go to the low state if the estimated time error of the instrument is worse than +500ms and will also stay in the high state after initial turn-on until the data on the parallel output lines are correct. This line, therefore, provides one line which, when in the low state indicates that the time data is "OK" to read. To convert the Model 60-DC to this configuration on the 1kHz line, remove the bottom cover of the instrument and locate assembly 86-44. For identification of this Assembly and its parts, see Figure 3-4 of this manual. Locate the jumper wires (looks like a ¼ watt resistor with one black band) labeled JPR3. Unsolder the end connected to the hole labeled "A" and solder it into the hole labeled "B". Unsolder the jumper marked JPR2 and remove it from the board. In the place of JPR2, solder in a 33kΩ resistor (¼ watt ±5%

carbon resistor preferred). Replace the cover and the screws, the conversion is now complete.

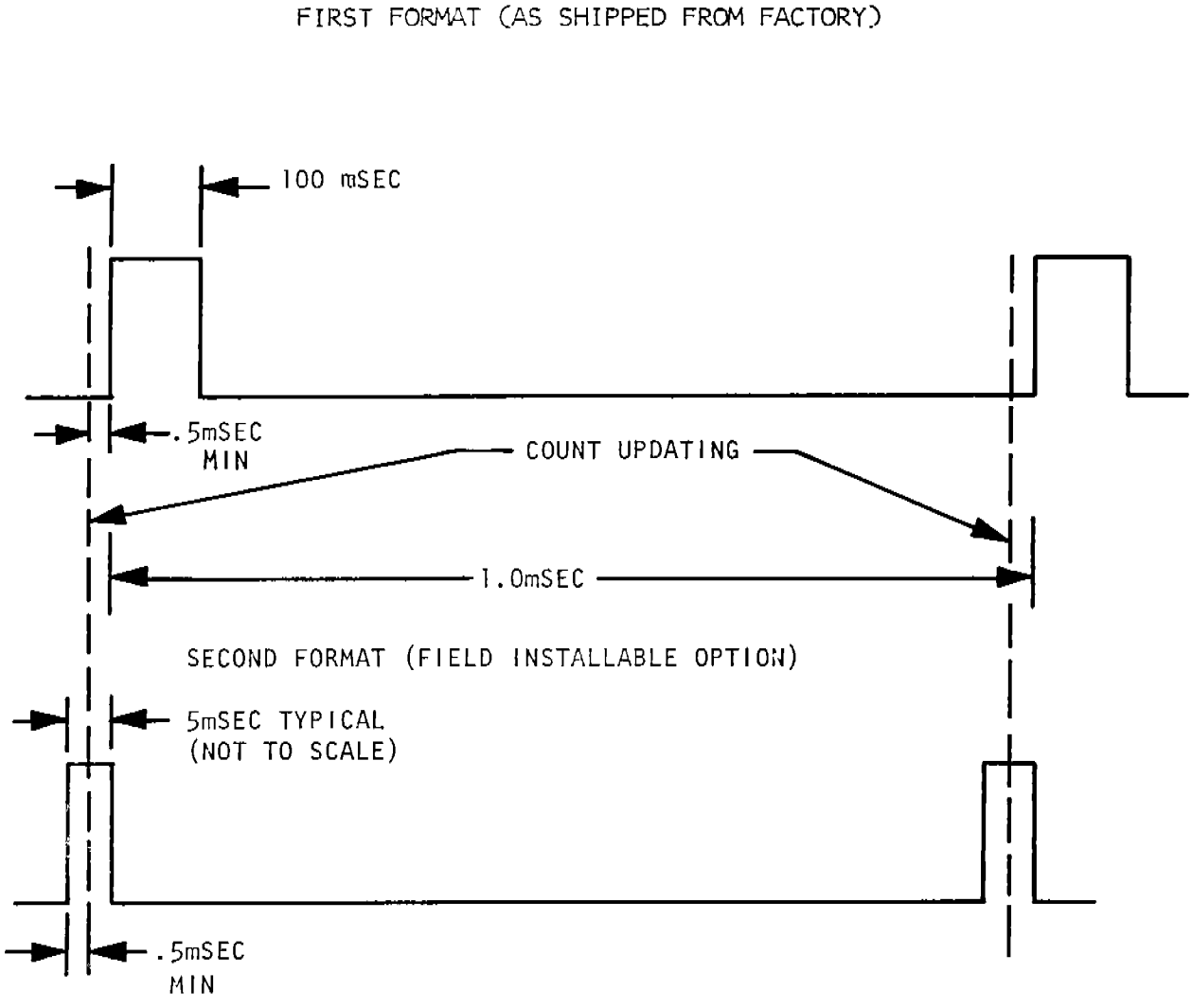


FIGURE 3-3 MILLISECOND COUNTER TIMING DIAGRAM 1kHz SIGNAL SHOWN PIN 9 OF OUTPUT CONNECTOR

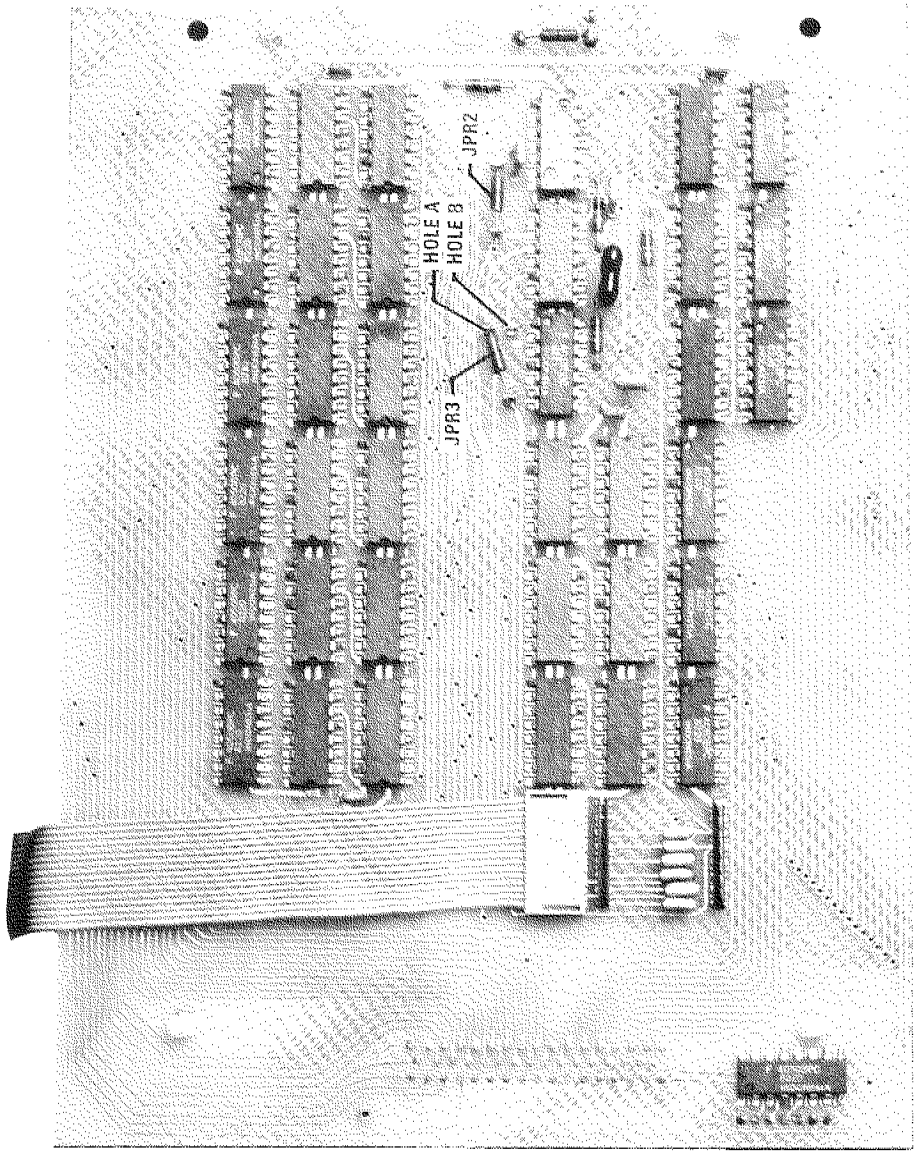


FIGURE 3-4 PARTS LOCATION - PARALLEL BCD OUTPUT OPTION

SECTION IV

THEORY OF OPERATION

4-1 BLOCK DIAGRAM - MODEL 60-DC

4-2 Refer to Figure 4-1 below to assist in the clarification of the overall operation of the Model 60-DC as described here.

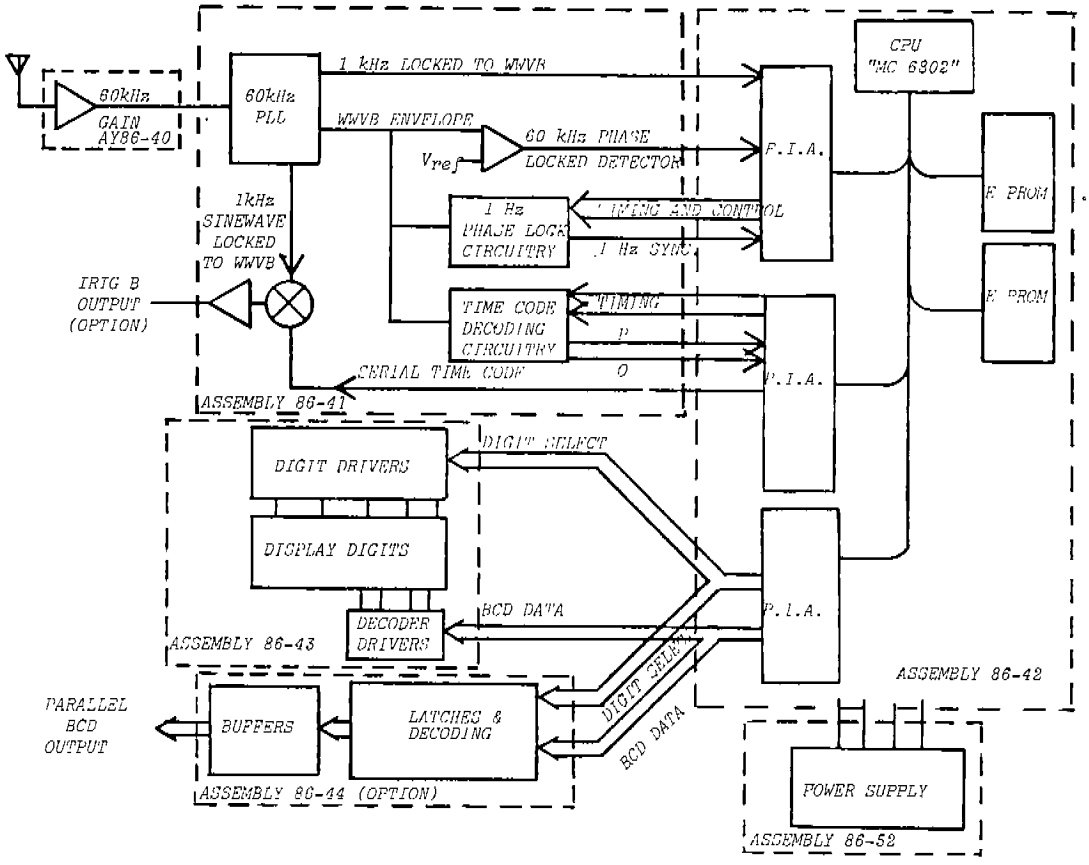


FIGURE 4-1 BLOCK DIAGRAM - MODEL 60-DC

4-3 The Model 60-DC has been designed to provide time information synchronized with the National Bureau of Standards. This is done by reading the time code signal

transmitted by radio station WWVB and using this time information to initially set the clock and using the carrier frequency to derive the clock rate.

4-4 As an overview, the Model 60-DC consists of several peripheral blocks operating under the control of the central processor, a Motorola MC6802.

4-5 The Digital Board, Assembly 86-42, consists mainly of program storage memory, read-write data storage memory, interface circuits and the 6802 processor. This central processor is capable of communicating with the other functional blocks, receiving data and transmitting control signals. This results in synchronizing the time outputs with the signal as transmitted by WWVB.

4-6 In synchronizing the time with the WWVB signal, there are two tasks. First, synchronizing the local standard with the WWVB seconds, and second, decoding the time code received. These functions are accomplished by two-way communication between the Analog Board, Assembly 86-41, and the Digital Board.

4-7 Contained on the Analog Board is the circuitry for synchronizing the local seconds with those of the received carrier. This 1 Hz sync circuitry, under the control of the processor, sends a pulse coincident with the WWVB second to the central processor. This pulse is generated after averaging approximately 50 seconds of code.

4-8 Also, contained on the Analog Board is the 60 kHz phase lock loop. This circuit provides the timing to keep the time scale locked to NBS time after the current time has initially been determined. The decoding circuitry sends the processor the code value for each second. Thus, the processor can determine if each second was a "0", "1", or ten-second marker "P".

4-9 Provisions have been made on the Analog Board for providing a rear panel output capable of driving a remote display (using an IRIG B format). This output code is generated on the Digital Board in a level shift form and sent to the Analog Board where it amplitude modulates a 1 kHz sine wave carrier.

4-10 The Display Board, Assembly 86-43, under the control of the processor, displays the decoded time. The Display Board operates in a multiplexed mode with left and right digit information.

4-11 Parallel BCD Time output, RS-232 C and IEEE-488 Interface are available on special order. They are added to the Model 60-DC as an additional circuit board. These assemblies utilize the same data as the display and proper synchronizing signals. Please note that only one of these three options may be installed on any clock.

4-12 R.F. BOARD - ASSEMBLY 86-40

4-13 The WWVB receiver circuit board supplies power to the active antenna and provides a controllable gain at 60 kHz. The bandwidth is about ±1 kHz, with two tuned stages and maximum gain at 60 kHz of 85 db.

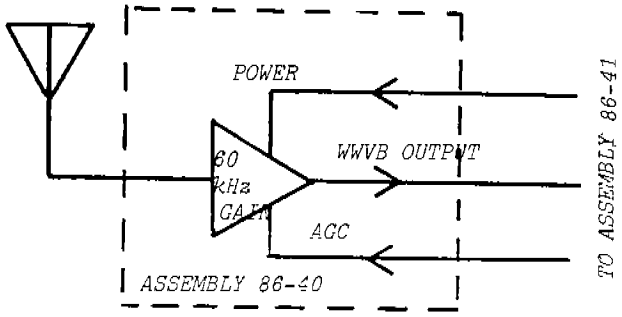


FIGURE 4-2 WWVB RECEIVER, R.F. BOARD

4-14 ANALOG BOARD - ASSEMBLY 86-41

4-15 The theory of operation of the Analog Board may best be understood by referring to the block diagram and the Assembly 86-41 Schematic in Section 6-6 of this manual.

4-16 U_1 constitutes a 60 kHz gain stage with a fixed gain of 45 db. The output of U_1 is rectified, filtered, and fed back to the gain control input of the R.F. Board 86-40. This AGC loop maintains the output of U_1 at .5 to 1.5V RMS over an antenna input signal range of 0.1 mv to 10^5 µ v.

4-17 The output of U_1 goes to the 60 kHz PLL comprised of the 7.68 MHz VCXO, the divider chain U_5 and U_7, the phase detector U_3 and U_4 and the loop filter U_9. The control range of the VCXO is ±6 ppm. U_5 is used to divide the 7.68 MHz.

signal by 128 and 64 to give 60 kHz and 120 kHz. The exclusive OR gate U_6 provides a 90° phase shifted output at 60 kHz which drives the balanced mixer U_3. This signal feeds a balanced to single ended converter U_{4D} whose output saturates at ±30° (under clean signal conditions). U_9 is the loop filter with R_{43}, R_{44}, and C_{15} chosen to give values of $\omega n = .25$ radians/second, $\zeta = 1.7$ for clean signal and $\omega n = .08$ radians/second, $\zeta = .6$ for noisy signal conditions. The VCXO also provides processor system timing (3.84 mHz).

4-18 The bias and symmetry controls consist of trim pots, R_{40} and R_{46}. These controls serve to null the drift rate of the loop filter under noisy and no signal conditions.

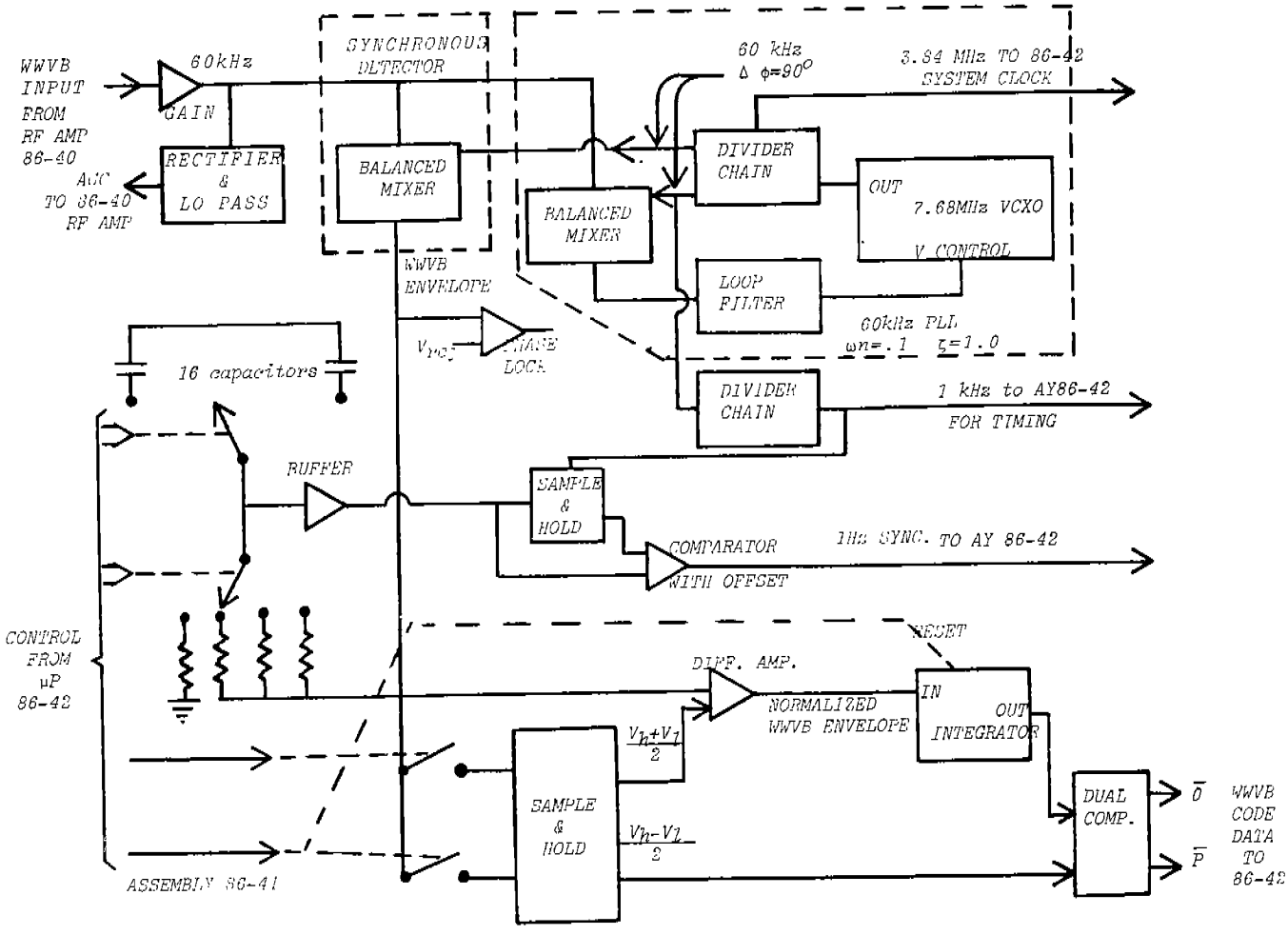


FIGURE 4-3 ANALOG BOARD - ASSEMBLY 86-41

4-19 The in-phase 60 kHz output from the divider chain goes to a second balanced mixer U_2. This mixer functions as a synchronous detector with its balanced output converted to single-ended by U_{4C}. R_{23}, the envelope bias adjust sets the WWVB envelope output to Zero (referenced to +5 volts) for no signal input.

4-20 WWVB Phase lock detection is accomplished by U_{4B}. This stage compares the filtered envelope voltage with a fixed reference level to determine if phase lock is maintained with WWVB. A low output on Pin #7 indicates phase lock.

4-21 The output of U_8 is a 1 kHz waveform phase-locked to WWVB. This waveform goes to the Digital Board 86-42 and is counted, forming the basic timing for the clock.

4-22 To obtain 1 Hz synchronization the WWVB envelope is sampled by a bank of capacitors, implemented by analog multiplexers $U_{15}$and U_{16}. Reference to Figure 4-4 may aid in clarification of this function.

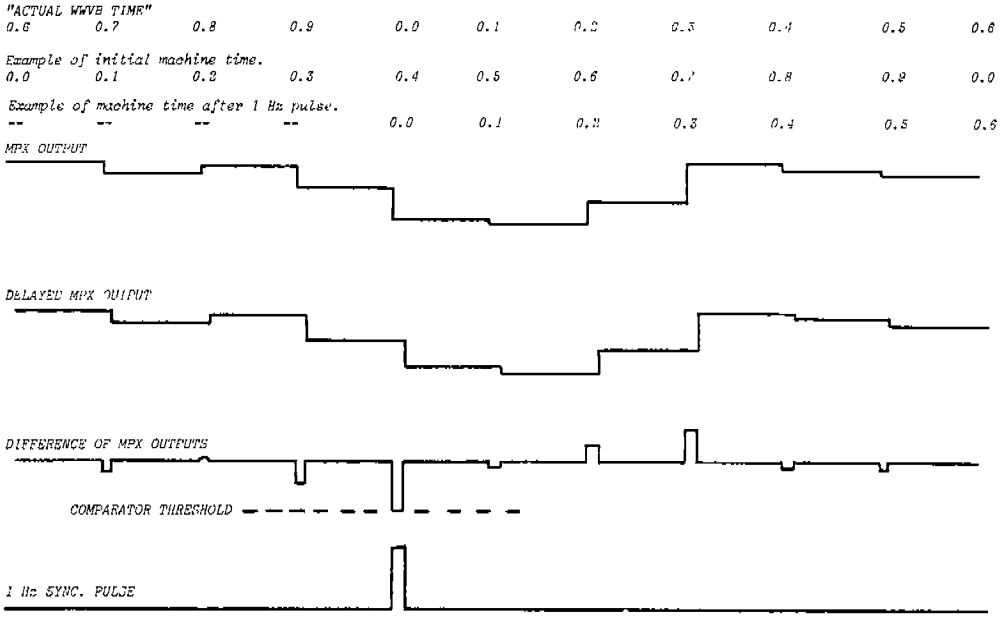


FIGURE 4-4 1 HZ SYNC. - TIMING DIAGRAM

4-23 Figure 4-4 represents the action of the 1 Hz sync. circuit during Mode 1 operation. Mode 1 operation seeks to synchronize the clock to WWVB within +50 ms. During Mode 1, only 10 of the 16 capacitors are used. The WWVB envelope is repeatedly connected, through R_{75}, to each capacitor during the same tenth of the second for a total of about 40 scans. Each capacitor thus accumulates about 4 seconds of time connected to WWVB. The charge pattern, due to the WWVB signal, on the capacitors grows with each scan, while noise tends to average to zero.

4-24 The WWVB time code is such that the envelope is always high for 2/10ths second before the exact second and always low for 2/10ths of a second after the exact second. During the remaining time in any second it may be either high or low. It is this drop in envelope level which the 1 Hz synchronization circuitry seeks to find.

4-25 As the multiplexer repeatedly scans the capacitors, the charge pattern that builds reflects this drop in envelope; the capacitor that is scanned just before the drop occurs accumulates more charge than the capacitor scanned just after the drop in envelope level. This drop is detected by comparing the charge on each capacitor with that on the previous capacitor as remembered by the sample and hold U_{21}. When the difference exceeds a reference level, the 1 Hz sync. pulse generated informs the processor that the envelope drop has occurred.

4-26 The reference level for the above mentioned comparison is the sum of two parts. One is a fixed level and the other is proportional to the WWVB signal. The fixed level prevents false synchronization when the signal from WWVB is not present, while the proportional part enables the synchronization time to remain about constant regardless of the WWVB signal level.

4-27 A similar process is repeated when the scan step rate is increased to 10ms. and 1ms. to progressively refine the agreement of the clock time with that of the WWVB envelope drop. For the finer resolution scans, all sixteen capacitors are used. This allows extra margin for each scan window, which is needed when the WWVB second occurs at +5 scan steps from the clock second. It should be noted that this algorithm provides an effective signal bandwidth that is independent of the noise bandwidth, provided enough scans occur.

4-28 After the clock has been synchronized with the WWVB second, the time code stripper comes into play. Figure 4-5 depicts this time code recovery operation.

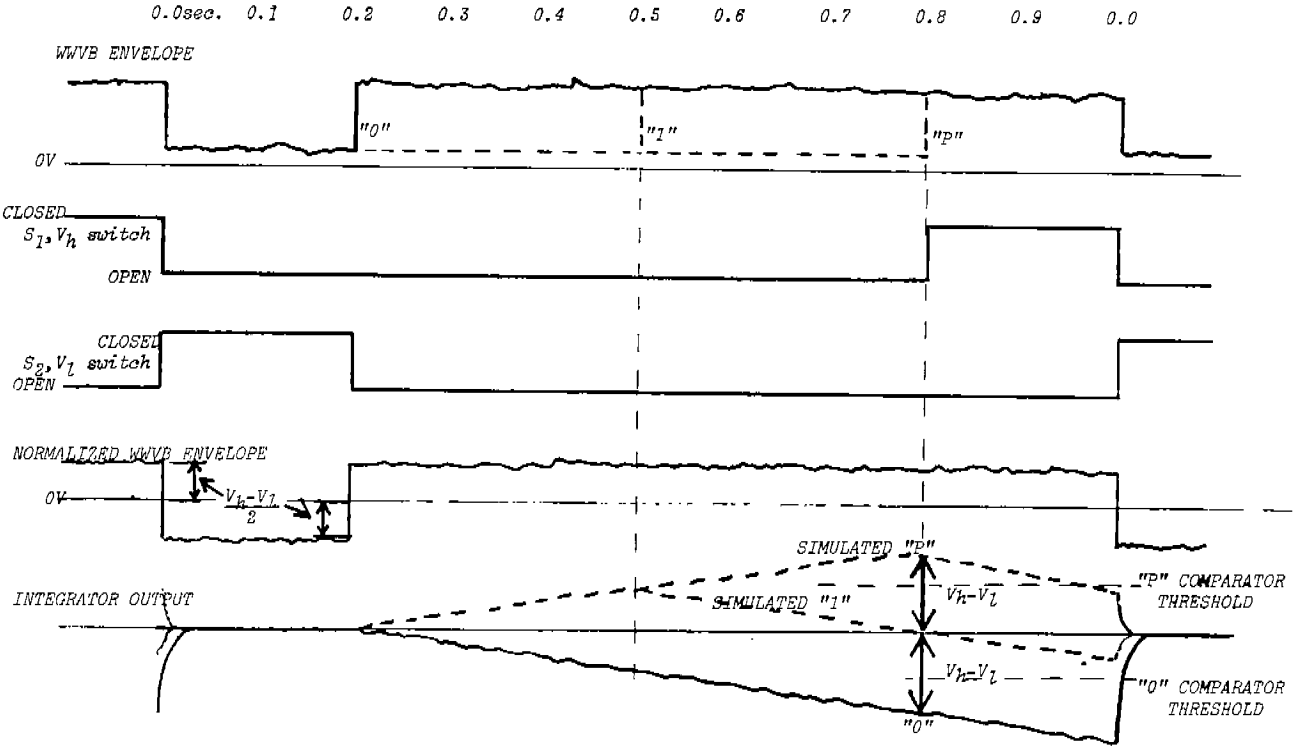


FIGURE 4-5 BLOCK DIAGRAM- TIME CODE RECOVERY

4-29 U_{13B} AND U_{13C} respectively sample the high and the low portions of the WWVB envelope. This sampling produces averaged high and low values of V_H and V_L. The difference between V_H and V_L is the basic measure of signal level used to derive the time code.

4-30 The mean value of V_H and V_L is used in conjunction with the WWVB envelope to produce a voltage shifted version of the envelope. This signal swings equally in both directions about the reference level. This "normalized envelope" drives an integrator which is reset from .0 to .2 of each second. From .2 to .8

seconds, the time code information is transmitted and the integrator weights it all equally. At time .8 seconds, the output of the integrator constitutes a best estimate of the value of the current seconds code character. Digitizing of this estimate is done by comparison with V_H-V_L in an effort to eliminate signal level dependence.

4-31 Since the integration time constant is ¼ the integration interval, the integrator output at 0.8 seconds is -4X(Normalized Envelope Voltage) in the absence of noise. The "Normalized Envelope Voltage" is the signal at pin 7 of U_{10B}. This amounts to 2 (V_H-V_L) for a "P", zero for a "1" and -2(V_H-V_L) for a logic "0". The reference level for the "P" comparator is +(V_H-V_L) and for the "0" comparator is -(V_H-V_L). These levels are automatically midway between the levels they are meant to distinguish.

4-32 R_{69} is provided as a "1" bias adjustment which allows nulling of the offset voltages of U_{10B} and U_{12D}.

4-33 U_{11} is an output buffer used to convert the 0 to 10V op. amp. outputs to 0 to 5V logic levels for use by the Digital Board. U_{17} and U_{18} are used as input buffers which condition the Digital Board outputs to a 0 to 10V swing as required by the Analog Board.

4-34 DIGITAL BOARD ASSEMBLY 86-42

4-35 See Section VI for schematic of the digital board. The digital board utilizes a M6802 microprocessor as the central processor. The processor controls data flow over a multiline bus in a typical microprocessor configuration as a controller, stored program memory, read write data memory, and input/output interface. U2, U3, U4 are the I/O interface devices. All communications with the other areas flow through them. U12, U13 are type 2114 rams and comprise the read/write memory used for storage of program variables. U5, U7, 2716 e-proms are used for program storage. U9, U10, U11, U15, TTL, MSI chips perform address decoding to direct data flow to and from the proper devices. U14 generates a reset pulse to ensure orderly start of operating at turn on.

4-36 The function of the 86-42 board is determined within a wide range, by the program stored in U5-U8. It is beyond the scope of this document to describe in detail the operation of this program, however, a general outline is provided in the software section to aid in understanding of the clock's behavior.

4-37 U_2, U_3, and U_4 are Motorola MC6821's (PIA's) which are used to interface the constantly changing buss lines to the external portions of the Model 60-DC.

4-38 Timing is generated within the 6802 which divides the 3.84MHz input clock signal by 4 and generates the required timing signals.

4-39 U_{14} provides a reset signal on powering up the Digital Board while U_9, U_{10}, U_{11} and U_{15} perform address decoding.

4-40 If the reader is interested further in the operation of the microprocessor and its associated chips, he should refer to literature available from Motorola which more fully describes the operation of the MC6802.

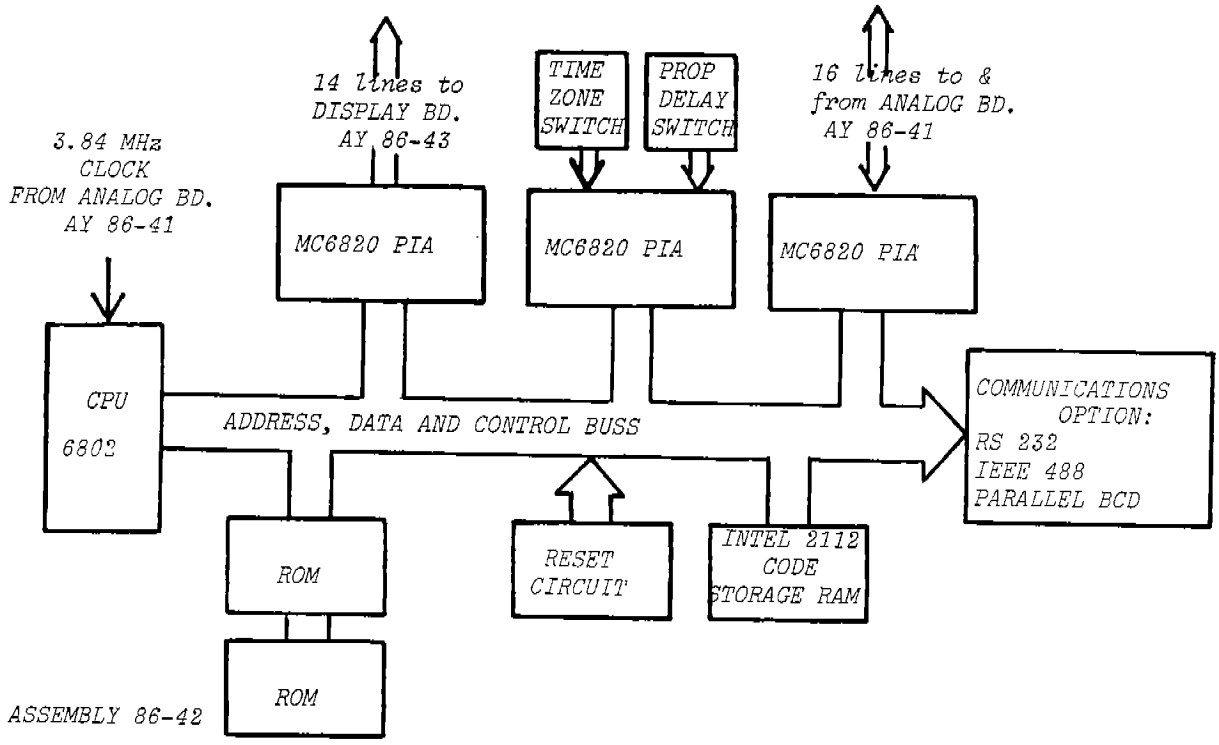


FIGURE 4-6 DIGITAL BOARD- ASSEMBLY 86-42

4-41 DISPLAY BOARD - ASSEMBLY 86-43

4-42 The display assembly is depicted in the block diagram, Figure 4-7 below. Each pair of digits is selected, one pair at a time. When a given pair is selected, the appropriate digits are presented (in BCD) to the 7-segment decoder drivers U_1 and U_2. These I.C.'s then illuminate the proper segments in the selected digit pair. Each millisecond, a new pair of digits is selected, making a complete scan in 5 milliseconds.

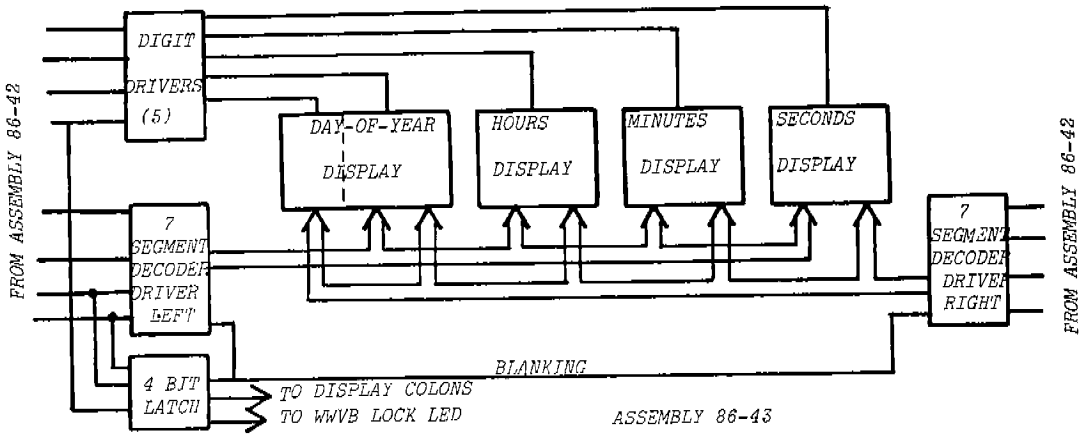


FIGURE 4-7 BLOCK DIAGRAM- DISPLAY BOARD

4-43 The left digit information associated with the hundreds of days is also used for control functions. It is used to control the WWVB "LOCK" LED, the colons, and the blanking of the display. These control functions are exercised via a 4 bit latch (U_3).

4-44 POWER SUPPLY

4-45 See Section VI for schematic of power supply assembly.

4-46 The power supply itself is a standard design and needs no explanation.

4-47 The reset circuit, U6, senses ripple on either of the +5V supplies and generates a negative going pulse which goes to the reset flip-flop on Assembly 86-42, forcing a program reset as long as ripple is resent on either +5V line. This protects against erratic operation during times of low line voltage.

4-48 REMOTE DISPLAY DRIVING (IRIG B)

4-49 The Remote Display (IRIG B Time Code) is generated on the Digital Board in a level shift form and converted to an amplitude modulated 1kHz form on the Analog Board.

4-50 The 1kHz carrier is generated by means of a weighted sum of 10 outputs from U_8, each of which goes high for 100 µsec. in each millisecond. Through suitable weighting of the contribution of each successive 100µ sec. interval, an approximateion of a 1kHz sinewave results. Low pass filtering removes most of the harmonics created by this generation technique. U_{23} modulates this carrier and since both the carrier and modulation are synchronous with the WWVB signal, they are synchronous with each other. Modulation level changes occur at positive zero crossings of the carrier, insuring a glitch-free output.

4-51 The Model 60-DC is delivered with the IRIG B code output in the amplitude modulated 1kHz format. To change to a level shift format, remove the lid and locate the two switches in the right rear corner of the analog board (86-41). Note that only one switch is to be on at a time. For a level shifted form, turn off "AM" and turn on "TTL".

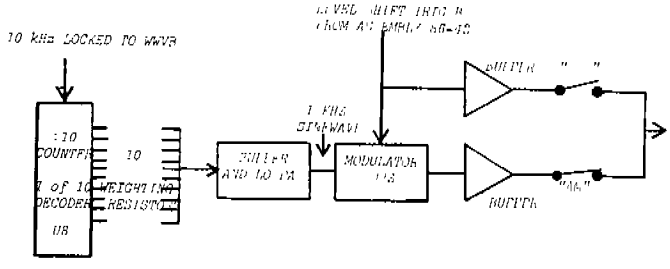


FIGURE 4-8 BLOCK DIAGRAM- REMOTE DISPLAY DRIVING OPTION

4-52 PARALLEL OUTPUT OPTION ASSEMBLY 86-44

4-53 The parallel output option provides logic level output of the same time as shown on the display. It does this by demultiplexing the display data lines and latching the data in a buffer consisting of U19-U27. On the second, the data in this buffer is strobed into the out-

put buffer, U10-U18. The data in the output buffer is sent to the outside world thru drivers U1-U9 to provide increased drive capability.

4-54 A millisecond counter, U31-U33, together with drivers U28-U30, provide milliseconds output, and also control loading of time into the output buffer. This counter is synchronized with NBS time via the "time ok" line thru trigger latch U35.

4-55 The function of U37 and its associated circuitry, is to provide either an edge or a level for controllin sampling of the BCD output lines. U36 is an output driver for several miscellaneous outputs. A timing diagram, showing the relationship of the 1 kHz line to the data output lines is shown in Figure 3-3 to assist in reading th lines during the time when they are stable.

4-56 IRIG-H

4-57 IRIG-H Time Code is generated by the 6802 microprocessor. The signal path is thru U3 pin 39 and buffer transistor Q5. The voltage swing is 0 to 5V. The timing is described in Section XI .

SECTION V

MAINTENANCE AND TROUBLESHOOTING

5-1 MAINTENANCE

5-2 The Model 60-DC has been designed to provide maintenance free operation for many years. The instrument contains only seven adjustments, most of which will never require resetting. The adjustments are: two tunable coils in the R.F. Board, WWVB Envelope Bias, WWVB Phase Lock Bias, WWVB Phase Lock Symmetry and an adjustment for setting the VCXO center frequency.

5-3 Although it is highly unlikely that any of the adjustments in the Model 60-DC will require resetting for the life of the instrument, the procedure for each adjustment is included below. All of the following adjustments can be performed with an oscilloscope, a signal generator capable of outputting 60 kHz at about 1 mv and an antenna for receiving the signal from WWVB.

5-4 R.F. BOARD TEST (86-40)

1. Ground AGC line to 86-40 Board (green wire).
2. Inject 60kHz (AC coupled) into antenna input. Set the generator level such that the output just saturates - then reduce by ½.
3. Adjust cores for max. output.

5-5 ANALOG BOARD ALIGNMENT (86-41)

(Note: Analog Board Tests are performed with scope ground at +5VDC. Be sure scope is floating.)

5-6 ENVELOPE TRIM

With the signal input of the 86-41 Board shorted (pins 3 & 4) view T.P. AC with scope and adjust R23 for an output of -20mv. (scope reference @ +5VDC.)

5-7 VCXO ADJUSTMENT

Remove input ground and supply WWVB to antenna input. With T.P. AD on scope, set the ceramic trimmer (C22) for a voltage of -2V (with reference @ +5V) This adjustment should be done in very small steps allowing several seconds for the long time constant of the loop to stabilize. If

phase lock cannot be obtained by this method, it will be necessary to use a frequency counter to set the VCXO. Using a high impedance probe, attach probe to the collector of Q2(2369). Adjust the ceramic trimmer to provide 7,680,010Hz output on counter. The unit should now phase lock. (The long R-C time constant of the loop may be circumvented by a momentary short between T.P. "AD" and T.P. "AK", which discharges C15.) After phase lock, a slight adjustment of the trimmer will move the control voltage to the desired -2VDC level.

5-8 PHASE LOCK BIAS

While viewing T.P. AD, remove antenna and short pins 3 & 4 of Analog Board. Adjust R40 for zero volts drift (<100mv/min.)

5-9 PHASE LOCK SYMMETRY

Remove short from pins 3 & 4. Connect scope ground to T.P. AN and view T.P. AM with unit not phase locked. Adjust R46 for a symmetrical swing above and below the ground reference.

5-10 CODE BIAS ADJUSTMENT

Reconnect to antenna and allow unit to sync through Mode 5 - trigger scope on the rising edge of 1Hz (T.P. AE) and observe T.P. AF (scope reference +5VDC). Adjust trim pot R69 such that the "P"s are as high as the "Ø"s are low - and the "1"s should be at the reference level (+5V).

5-11 TROUBLESHOOTING

5-12 If a failure of the Model 60-DC occurs, it is recommended that the unit be returned to the factory for repair. Due to the nature of this microprocessor-based instrument, field repair by unfamiliar personnel may be very difficult. If it is not possible to return the unit to the factory the following section as well as the SCHEMATICS (SECTION VI) and THEORY OF OPERATION (SECTION IV) of this manual may be of assistance in locating the cause of a malfunction. First, we will cover the most common problem areas to assist in isolating general malfunctions and second, probable causes of various observed malfunctions will be covered.

5-13 ANTENNA INSTALLATION

5-14 As mentioned in Section 2-8 the most important, yet most overlooked factor in proper operation of the Model 60-DC is proper selection of a site and installation of the WWVB antenna. Without a proper antenna installation the signal from the transmitter will not be received and the unit cannot possibly function properly. in many cases "just to try it out" (when the A-60FS antenna is used) an attempt will be made to operate the unit with the antenna inside of a building. This, as often as not, results in inability to phase lock to the signal. In some cases phase lock may be obtained, but the low signal level in these cases will be too low for the unit to read the time code information. Thus, the display will not light or may require extremely long periods of time to read two time frames properly and turn on the display.

5-15 After the antenna installation has been completed, connect the instrument to the proper power source. Turn on the power switch and the colons should light, turn off for ½ second and on again, remaining on. Looking down in the display window,below each pair of digits should be a faint flickering light (display "keep alives"). This will indicate that the microprocessor is scanning the display assembly. Within 50 seconds the "WWVB LOCK" LED on the panel will light and within five minutes the display should light indicating the proper time. If any of the above indications fails to occur the following sections will be of assistance in locating the malfunction.

5-16 POWER SUPPLY

5-17 The first area to verify in any troubleshooting approach is that the power supply is operating properly and that no circuit board or component is drawing the supply voltage down. If no indication of operation is evident from the front panel, check to be certain that the AC source is operational. Next, remove and test the fuse on the rear panel. When these are determined to be operational, remove the top and bottom covers on the Model 60-DC and refer to Section VI forSchematics and Parts Lists of the Power Supply (Assembly 86-52).

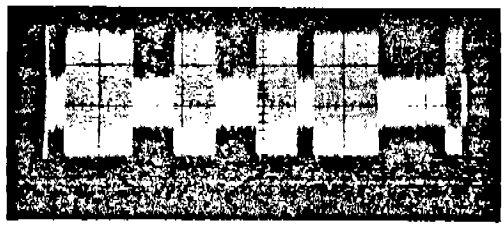
5-18 The output voltages from the power supply should be within ±5% of the specified values. A low supply voltage can be caused by a defective part on the Power Supply Assembly or by components in other parts

of the instrument drawing excessive power from the supply. Disconnect the flat cable connected to the power supply board and check the voltage again. If the supply voltage remains low, the problem is a component on the Power Supply Assembly. A common problem on other assemblies will be an integrated circuit which has failed and is drawing excessive current. These normally can be located by touch since they will be very hot. Disconnection of each circuit assembly in turn may aid in locating an assembly which is drawing excessive power.

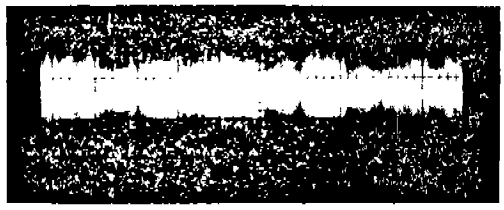
5-19 Too high a voltage noted on a power supply output is an indication that a problem exists on the Power Supply Board.

5-20 WWVB SIGNAL

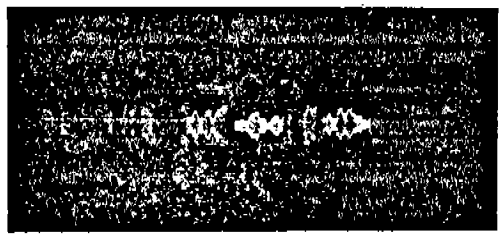
5-21 If the power supply is operating properly, the colons light and the keep alives are flickering (a solid light in only one or two is an indication of improper microprocessor operation), the WWVB signal as seen by the receiver should be checked. This WWVB signal can be viewed with an oscilloscope connected to T.P. AJ in the left rear corner of Assembly 86-41. The WWVB signal, more fully described is Section IX of this manual, consists of a 60 kHz R.F. carrier which is amplitude modulated, dropping in level by 10 db once/second. On the next page are pictures of this signal in a very clean state and a state showing a very noisy condition. When viewing the 60 kHz carrier on the scope you must be able to vaguely see the 60 kHz carrier with the 1 Hz drop in carrier level. If this can be seen through local noise interference, the 60-DC will be able to decode the time information. If only hash and noise spikes at random times and rates are seen, it can be certain that the antenna or R.F. assembly are not operating properly. See Section 5-5 for a description of the alignment procedure for the R.F. Receiver which will check it for operation. The antenna operation can be checked as described in Sections VII.



VERY CLEAN WWVB SIGNAL



POOR SIGNAL FROM WWVB



SIGNAL FROM WWVB NOT VISABLE - NOISE ONLY

5-22 MICROPROCESSOR ASSEMBLY

5-23 The first indication that the Digital Board-Assembly 86-42 is not operating properly is that the keep alives in the display will not be flickering. One or two will be bright spots and the remaining will not be lit, the problem lies in the Assembly 86-42. The first area to check is that the assembly is receiving its "clock". This comes from the Analog Board and is supplied on Pin L. This pin should have a 3.84 MHz TTL level signal. The 7.68 MHz oscillator can be seen on Assembly 86-41, U_5 Pin #1. The second area to examine for failure

is the 1 kHz which comes from the Analog Board on Pin X. This 1 kHz interrupt has a 90% duty cycle. If it is found that both the 1 kHz and 3.84 MHz signal are operating properly and the display keep alives do not flicker, the problem lies in the Digital Board. Check this assembly to be certain that the I.C.'s are tight in the socket and that there are no shorts on the board. It is possible that conductive lint could short between the close traces on this board. Further troubleshooting of this assembly should be referred to those familiar with the operation of microprocessors.

5-24 ANALOG BOARD

5-25 If the above mentioned sections appear to be operating properly, a brief inspection of various sections of the Analog Board may isolate the difficulty. Look at the WWVB envelope with a scope. Connect a scope to test point "AC" and connect the scope ground to the tab of the 5 volt regulator (U24) in the left rear corner of this assembly. (Make sure that the scope is floating.) This signal may have noise super-imposed and will drop from high to low on the second. Interfering signals will not generally have a code on them which will make them distinguishable from the WWVB signal.

5-26 If the unit has lost phase lock and the signal from WWVB is present, the phase lock can be adjusted as described in Section 5-7 of this manual. When this unit has phase locked to WWVB the 1 Hz lock can be checked. With the scope triggered by T.P. "AE", look at the WWVB envelope T.P. "AC". This envelope should drop in level 0.2 seconds after the sweep starts. Watch the 1 Hz sync. progress to higher precision by watching the output of U_{20} Pin #6 (CA3130). After initial turn-on this should hop around in 0.1 second steps for about a minute. It should then reset to +5 volts reference and another scan of 10ms. steps should build up right around the 0.0 second. After another minute, it resets and the 1.0ms./step starts. This takes longer, and times out to reset at 2 minutes if this level of sync. is not achieved.

5-27 With all of the above functioning as described, the unit will turn on displaying the correct time. Below is a list of possible observed symptoms and their related causes to assist in isolating specific problems.

5-28 SYMPTOMS AND POSSIBLE CAUSES

5-29

1. "WWVB LOCK" LED does not light
   a. Poor antenna installation causing lack of signal. See Section 5-13.
   b. Analog Board Alignment
   c. Other integrated circuits in the above areas not properly operating. This could be detected by inability to make adjustments specified above.
   d. LED defective

2. "WWVB LOCK" LED remains on for over 15 seconds after the antenna is disconnected.
   a. Envelope bias trim pot incorrectly adjusted, see Section 5-6.

3. When the unit is turned on the colons do not light.
   a. Unit not connected to power source.
   b. Fuse blown.
   c. Power Supply failure, see Section 5-16.
   d. Digital Board not functioning, see Section 5-22.
   e. Broken wire to the Display Board Assembly.
   f. Two or more LED's in the display not operational.

4. Unit turns on properly as described, after a period of operation the display goes off (one digit may remain lit) and the keep alives are not flickering.
   a. Failure as described in Section 5-22 caused by heat build-up in the instrument or in one I.C..

5. When the unit is turned on the "WWVB LOCK" LED lights properly, the colons light, but the display never turns on indicating the time.
   a. Analog Board Alignment. (check 1 Hz sync.)

6. When unit "Times In", the display lights properly but digits displayed are not correct (every other digit incorrect or like segments not lighting properly).
   a. If a wire to the Display Board from the Digital Board is broken, the same bit of

every other digit will be affected.

b. If the display drivers (DM8880) are not operating the same segments of every other digit will not be operating.

c. If only one segment of one digit is not operating, that segment may be burned out. This can be seen visually.

7. If the display blinks (after 24 hours), this is an indication of not remaining phase locked to the transmitter. See Section 3-8 for proper operational description of this feature.
   a. Analog Board Alignment, see Section 5-5.

8. Parellel Time Output lines are not correct. These lines should agree with the display as they are driven in parellel with the display.
   a. See Parellel BCD Putput option Schematic in Section III and trace defective lines to find inoperative I.C. or other failure on Assembly 86-44.

9. Remote Display Driving Output (IRIG B) inoperative.
   a. Check to see that a level shift IRIG B code is coming from Assembly 86-42 to Assembly 86-41 on Pin #R of the edge connector.
   b. Check U_{17}, U_{22} and U_{24} for proper operation.
   c. Be sure that either IRIG B switch is on, but not both.

5-30 This concludes the Troubleshooting Section of the manual. If the above information has not resulted in repair of the instrument, please contact the factory for assistance.

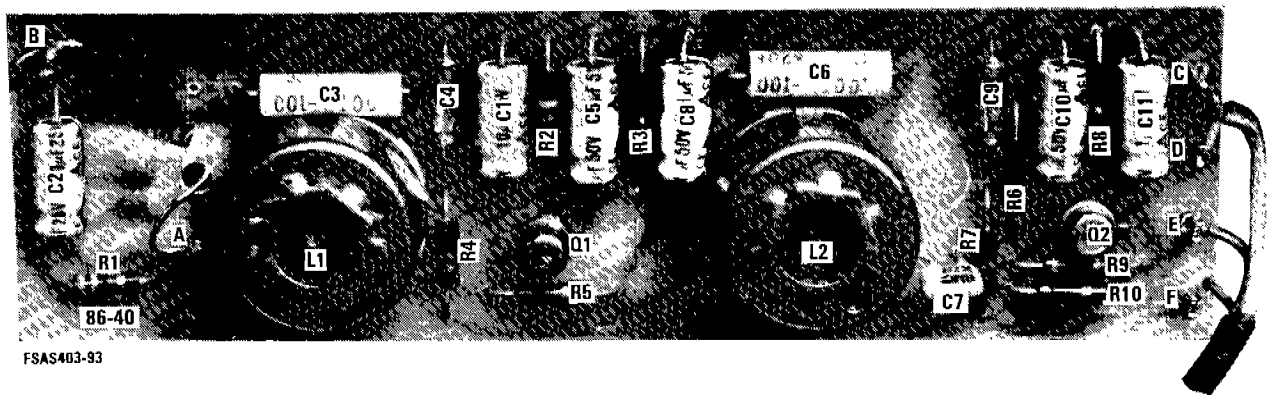
SECTION VI

SCHEMATICS AND PARTS LIST — MODEL 60-DC

FSAS403-85

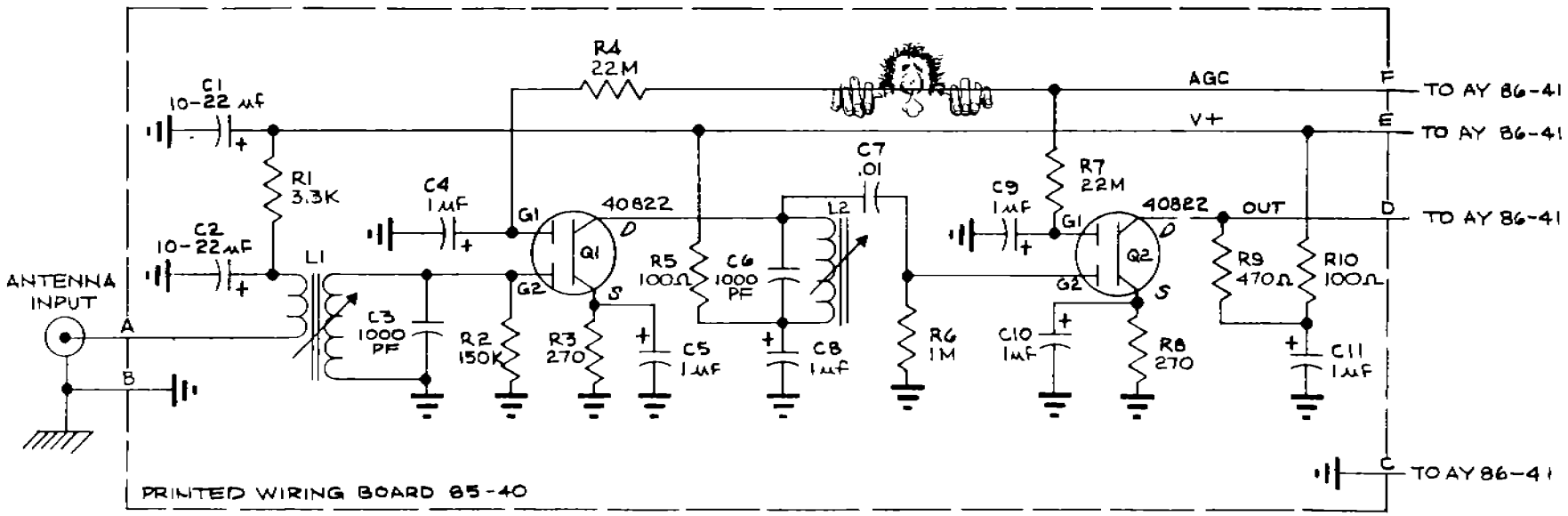
6-1 SYMBOL DESIGNATION REFERENCE 86-40

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	27-8-25	Cap. Alum Electro, 10uf 25V*
C2	27-8-25	Cap. Alum Electro, 10uf 25V*
C3	24-1	Cap. Polystyrene 1000pf
C4	32-29	Cap. Tant. 1uf
C5	27-1-50	Cap. Alum Electro, 1uf 50V**
C6	24-1	Cap. Polystyrene 1000pf
C7	36-83	Cap. Monolithic .01uf
C8	27-1-50	Cap. Alum Electro, 1uf 50V**
C9	32-29	Cap. Tant. 1uf
C10	27-1-50	Cap. Alum Electro, 1uf 50V**
C11	27-1-50	Cap. Alum Electro, 1uf 50V**
	*Cap.Tant. 22uf 15V can be used **Cap.Tant. 1.0uf 15V can be used	
L1	42-3	Coil R.F. Assembly
L2	42-2	Coil R.F. Assembly
PWB	85-40	Printed Wiring Board
Q1	175-1	RCA #40822
Q2	175-1	RCA #40822
R1	2-85	Res. Carbon 3.3K
R2	2-125	Res. Carbon 150K
R3	2-59	Res. Carbon 270ohms
R4	2-177	Res. Carbon 22M
R5	2-49	Res. Carbon 100ohms
R6	2-145	Res. Carbon 1.0Meg
R7	2-177	Res. Carbon 22Meg
R8	2-59	Res. Carbon 270ohms
R9	2-65	Res. Carbon 470ohms
R10	2-49	Res. Carbon 100ohms
	Note. All Resistors are ½W±5%	

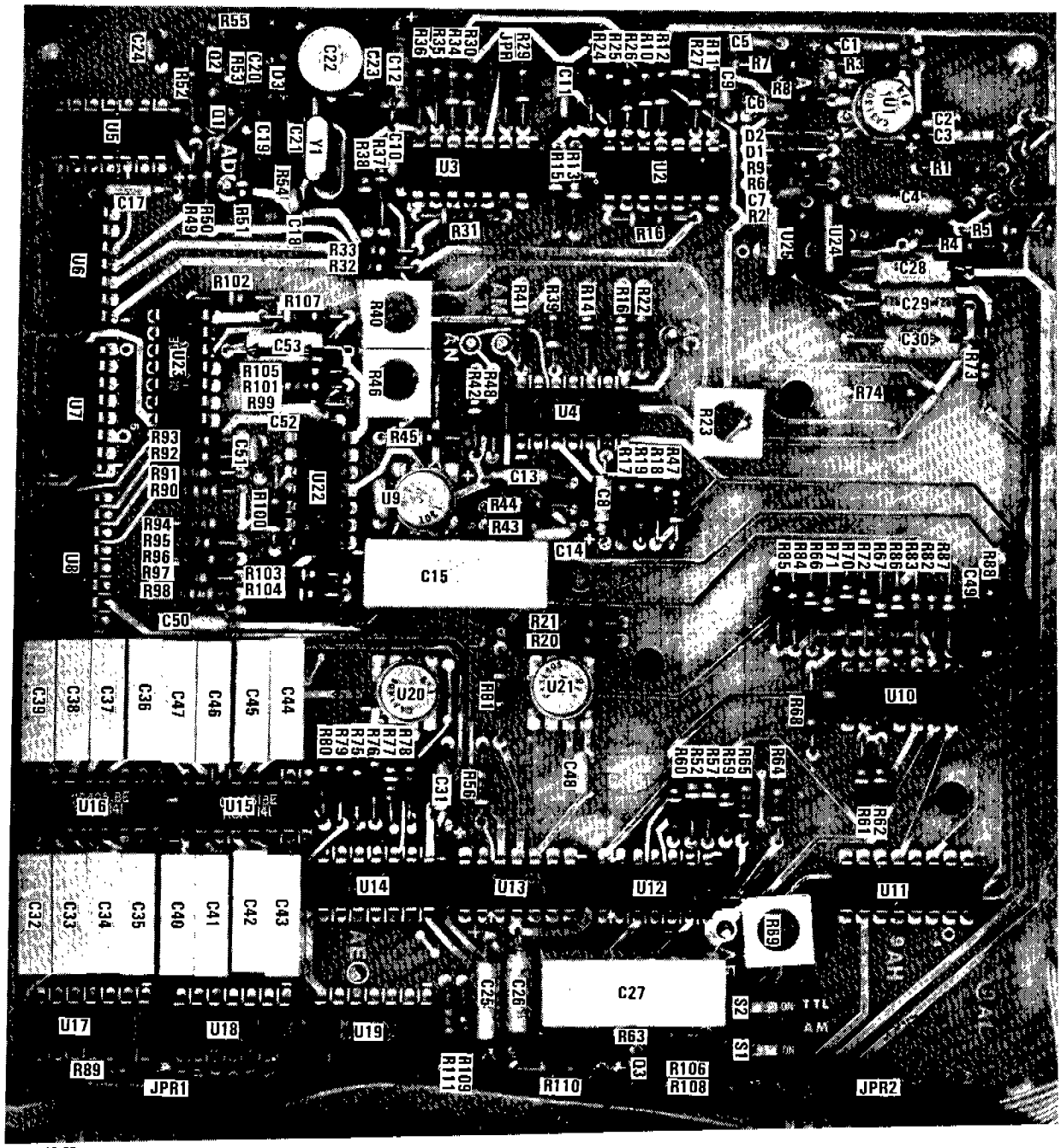


FSAS403-93

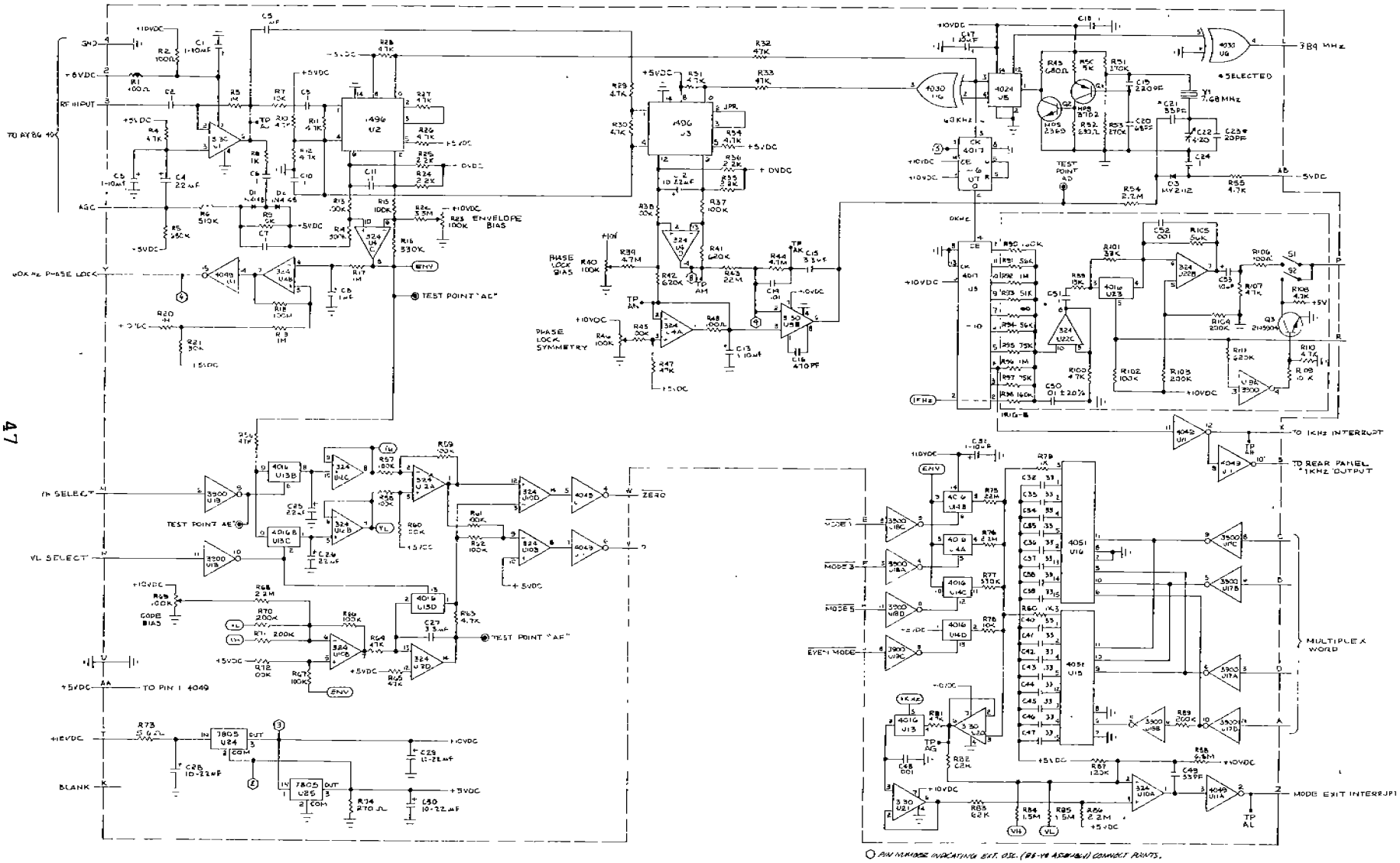
6-2 PARTS LOCATION-ASSEMBLY 86-40



6-3 SCHEMATIC-ASSEMBLY 86-40


R55
C24
C22
C23
C12
R30
R34
R35
R36
R29
JPR
R24
R25
R26
R10
R12
R27
R11
C5
C1
R3
R7
C9
C11
R8
C6
D2
D1
R9
R6
C7
R2
U1
C2
C3
R1
C4
R5
R4
C28
C29
C30
R73
R74
U24
U25
R23
U5
U6
U7
U8
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U2
U3
U4
U9
U10
C13
C14
C15
C27
C50
C51
C52
C53
C49
C48
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
R21
R20
R81
R68
R63
R89
JPR1
JPR2
S1
S2
TTL
AM

FSAS403-90



47

6-5 SCHEMATIC-ASSEMBLY 86-41

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	27-8-25	Cap. Alum Electro, 10uf 25V*
C2	36-95	Cap. Monolithic, 0.1uf
C3	27-8-25	Cap. Alum Electro, 10uf 25V*
C4	32-45	Cap. Tant 22uf 15V
C5	36-95	Cap. Monolithic, 0.1uf
C6	36-95	Cap. Monolithic, 0.1uf
C7	36-95	Cap. Monolithic, 0.1uf
C8	32-29	Cap. Tant 1.0uf 15V
C9	36-95	Cap. Monolithic, 0.1uf
C10	36-95	Cap. Monolithic, 0.1uf
C11	36-95	Cap. Monolithic, 0.1uf
C12	27-8-25	Cap. Alum Electro, 10uf 25V**
C13	27-8-25	Cap. Alum Electro, 10uf 25V*
C14	36-83	Cap. Monolithic, .01uf
C15	28-43	Cap. Polyester 3.3uf
C16	36-50	Cap. Monolithic 470pf
C17	27-8-25	Cap. Alum Electro, 10uf 25V*
C18	36-95	Cap. Monolithic, 0.1uf
C19	29-41	Cap. Dipped Mica 220pf
C20	29-29	Cap. Dipped Mica 68pf
C21	29-20	Cap. Dipped Mica 33pf
C22	33-20	Cap. Cer. Trimmer 4/20pf
C23	29-15	Cap. Dipped Mica 20pf
C24	36-95	Cap. Monolithic, 0.1uf
C25	32-45	Cap. Tant 22uf 15V
C26	32-45	Cap. Tant 22uf 15V
C27	28-43	Cap. Polyester 3.3uf
C28	27-8-25	Cap. Alum Electro, 10uf 25V**
C29	27-8-25	Cap. Alum Electro, 10uf 25V**
C30	27-8-25	Cap. Alum Electro, 10uf 25V**
C31	27-8-25	Cap. Alum Electro, 10uf 25V*
C32	28-19	Cap. Polyester .33uf
C33	28-19	Cap. Polyester .33uf
C34	28-19	Cap. Polyester .33uf
C35	28-19	Cap. Polyester .33uf
C36	28-19	Cap. Polyester .33uf
C37	28-19	Cap. Polyester .33uf
C38	28-19	Cap. Polyester .33uf
C39	28-19	Cap. Polyester .33uf
C40	28-19	Cap. Polyester .33uf
C41	28-19	Cap. Polyester .33uf
C42	28-19	Cap. Polyester .33uf
C43	28-19	Cap. Polyester .33uf
C44	28-19	Cap. Polyester .33uf
C45	28-19	Cap. Polyester .33uf
C46	28-19	Cap. Polyester .33uf
C47	28-19	Cap. Polyester .33uf
C48	36-58	Cap. Monolithic .001uf
C49	29-29	Cap. Dipped Mica 68pf
C50	36-83	Cap. Monolithic, .01uf
C51	36-95	Cap. Monolithic, 0.1uf
C52	36-58	Cap. Monolithic .001uf
C53	27-8-25	Cap. Alum Electro, 10uf 25V**

SYMBOL	TRUE TIME PART #	DESCRIPTION
D1	57-1	Diode 1N4148
D2	57-1	Diode 1N4148
D3	35-12	Varicap MV2112
JPR	317-12	Jumper, 12 wire
PWB	85-41	Printed Wiring Board
Q1	175-4	Transistor MPS 3702
Q2	175-3	Transistor MPS 2369
Q3	175-2	Transistor 2N3904
R1	2-49	Resistor, Carbon 100 ohms
R2	2-49	Resistor, Carbon 100 ohms
R3	2-145	Resistor, Carbon 1M
R4	2-89	Resistor, Carbon 4.7K
R5	2-141	Resistor, Carbon 680K
R6	2-138	Resistor, Carbon 510K
R7	2-97	Resistor, Carbon 10K
R8	2-73	Resistor, Carbon 1K
R9	2-97	Resistor, Carbon 10K
R10	2-89	Resistor, Carbon 4.7K
R11	2-89	Resistor, Carbon 4.7K
R12	2-89	Resistor, Carbon 4.7K
R13	2-121	Resistor, Carbon 100K
R14	2-132	Resistor, Carbon 300K
R15	2-121	Resistor, Carbon 100K
R16	2-133	Resistor, Carbon 330K
R17	2-145	Resistor, Carbon 1M
R18	2-203	Resistor, Carbon 100M
R19	2-145	Resistor, Carbon 1M
R20	2-145	Resistor, Carbon 1M
R21	2-108	Resistor, Carbon 30K
R22	2-157	Resistor, Carbon 3.3M
R23	20-7	Trim Pot., 100K(BEK-72PMR)
R24	2-81	Resistor, Carbon 2.2K
R25	2-81	Resistor, Carbon 2.2K
R26	2-89	Resistor, Carbon 4.7K
R27	2-89	Resistor, Carbon 4.7K
R28	2-89	Resistor, Carbon 4.7K
R29	2-89	Resistor, Carbon 4.7K
R30	2-89	Resistor, Carbon 4.7K
R31	2-89	Resistor, Carbon 4.7K
R32	2-113	Resistor, Carbon 47K

NOTE: All resistors are ¼watt±5%

* Cap.Tant 1.0uf 15V can be used
** Cap.Tant 22uf 15V can be used

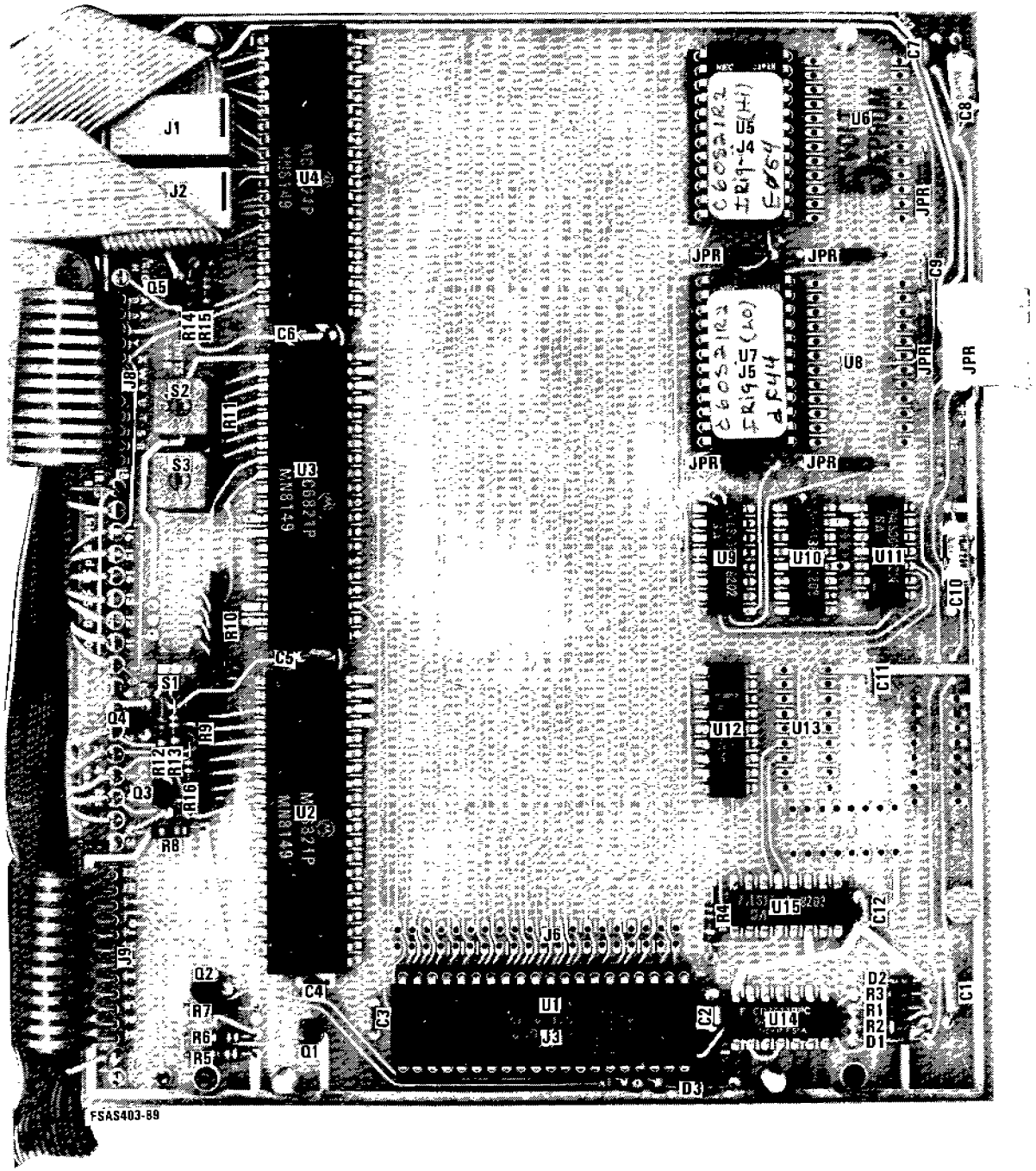
6-6 SYMBOL DESIGNATION REFERENCE 86-41

SYMBOL	TRUE TIME PART #	DESCRIPTION
R33	2-113	Resistor, Carbon 47K
R35	2-81	Resistor, Carbon 2.2K
R36	2-81	Resistor, Carbon 2.2K
R37	2-121	Resistor, Carbon 100K
R38	2-121	Resistor, Carbon 100K
R39	2-161	Resistor, Carbon 4.7M
R40	20-7	Trim Pot., 100K(BEK-72PMR)
R41	2-140	Resistor, Carbon 620K
R42	2-140	Resistor, Carbon 620K
R43	2-177	Resistor, Carbon 22M
R44	2-161	Resistor, Carbon 4.7M
R45	2-121	Resistor, Carbon 100K
R46	20-7	Trim Pot., 100K(BEK-72PMR)
R47	2-113	Resistor, Carbon 47K
R48	2-49	Resistor, Carbon 100 ohms
R49	2-69	Resistor, Carbon 680 ohms
R50	2-77	Resistor, Carbon 1.5K
R51	2-131	Resistor, Carbon 270K
R52	2-69	Resistor, Carbon 680 ohms
R53	2-131	Resistor, Carbon 270K
R54	2-153	Resistor, Carbon 2.2M
R55	2-89	Resistor, Carbon 4.7K
R56	2-113	Resistor, Carbon 47K
R57	2-121	Resistor, Carbon 100K
R58	2-121	Resistor, Carbon 100K
R59	2-121	Resistor, Carbon 100K
R60	2-121	Resistor, Carbon 100K
R61	2-121	Resistor, Carbon 100K
R62	2-121	Resistor, Carbon 100K
R63	2-89	Resistor, Carbon 4.7K
R64	2-113	Resistor, Carbon 47K
R65	2-113	Resistor, Carbon 47K
R66	2-121	Resistor, Carbon 100K
R67	2-121	Resistor, Carbon 100K
R68	2-169	Resistor, Carbon 10M
R69	20-7	Trim Pot., 100K(BEK-72PMR)
R70	2-128	Resistor, Carbon 200K
R71	2-128	Resistor, Carbon 200K
R72	2-121	Resistor, Carbon 100K
R73	2-19	Resistor, Carbon 5.6 ohms
R74	2-59	Resistor, Carbon 270 ohms
R75	2-177	Resistor, Carbon 22M
R76	2-153	Resistor, Carbon 2.2M
R77	2-133	Resistor, Carbon 330K
R78	2-97	Resistor, Carbon 10K
R79	2-73	Resistor, Carbon 1K
R80	2-73	Resistor, Carbon 1K
R81	2-89	Resistor, Carbon 4.7K
R82	2-116	Resistor, Carbon 62K
R83	2-116	Resistor, Carbon 62K
R84	2-149	Resistor, Carbon 1.5M
R85	2-149	Resistor, Carbon 1.5M
R86	2-121	Resistor, Carbon 100K
R87	2-123	Resistor, Carbon 120K
R88	2-165	Resistor, Carbon 6.8M
R89	2-128	Resistor, Carbon 200K
R90	2-126	Resistor, Carbon 160K
R91	2-115	Resistor, Carbon 56K
R92	2-145	Resistor, Carbon 1M
R93	2-114	Resistor, Carbon 51K
R94	2-115	Resistor, Carbon 56K
R95	2-118	Resistor, Carbon 75K
R96	2-145	Resistor, Carbon 1M
R97	2-118	Resistor, Carbon 75K
R98	2-126	Resistor, Carbon 160K
R99	2-101	Resistor, Carbon 15K
R100	2-89	Resistor, Carbon 4.7K
R101	2-109	Resistor, Carbon 33K
R102	2-121	Resistor, Carbon 100K
R103	2-128	Resistor, Carbon 200K
R104	2-128	Resistor, Carbon 200K
R105	2-115	Resistor, Carbon 56K
R106	2-49	Resistor, Carbon 100 ohms
R107	2-89	Resistor, Carbon 4.7K
R108	2-89	Resistor, Carbon 4.7K
R109	2-97	Resistor, Carbon 10K
R110	2-89	Resistor, Carbon 4.7K
R111	2-140	Resistor, Carbon 620K
S1	65-1	Switch 1 Pos.Dip
S2	65-1	Switch 1 Pos.Dip
U1	176-3130	I.C. RCA #C3130
U2	176-1496	I.C. Mot. MC1496L
U3	176-1496	I.C. Mot. MC1496L
U4	176-324	I.C. Nat. LM324
U5	176-4024	I.C. RCA 4024
U6	176-4030	I.C. RCA 4030
U7	176-4017	I.C. RCA 4017
U8	176-4017	I.C. RCA 4017
U9	176-3130	I.C. RCA #C3130
U10	176-324	I.C. Nat. LM324
U11	176-4049	I.C. RCA 4049
U12	176-324	I.C. Nat. LM324
U13	176-4016	I.C. RCA 4016
U14	176-4016	I.C. RCA 4016
U15	176-4051	I.C. RCA 4051
U16	176-4051	I.C. RCA 4051
U17	176-3900	I.C. Nat. LM3900
U18	176-3900	I.C. Nat. LM3900
U19	176-3900	I.C. Nat. LM3900
U20	176-3140	I.C. RCA 3140(or 3130)
U21	176-3140	I.C. RCA 3140(or 3130)
U22	176-324	I.C. Nat. LM324
U23	176-4016	I.C. RCA 4016
U24	176-7805	I.C. FSC 7805UC
U25	176-7805	I.C. FSC 7805UC
Y1	59-7.680	Crystal 7.680MHZ

NOTE: All resistors are ¼watt ±5%

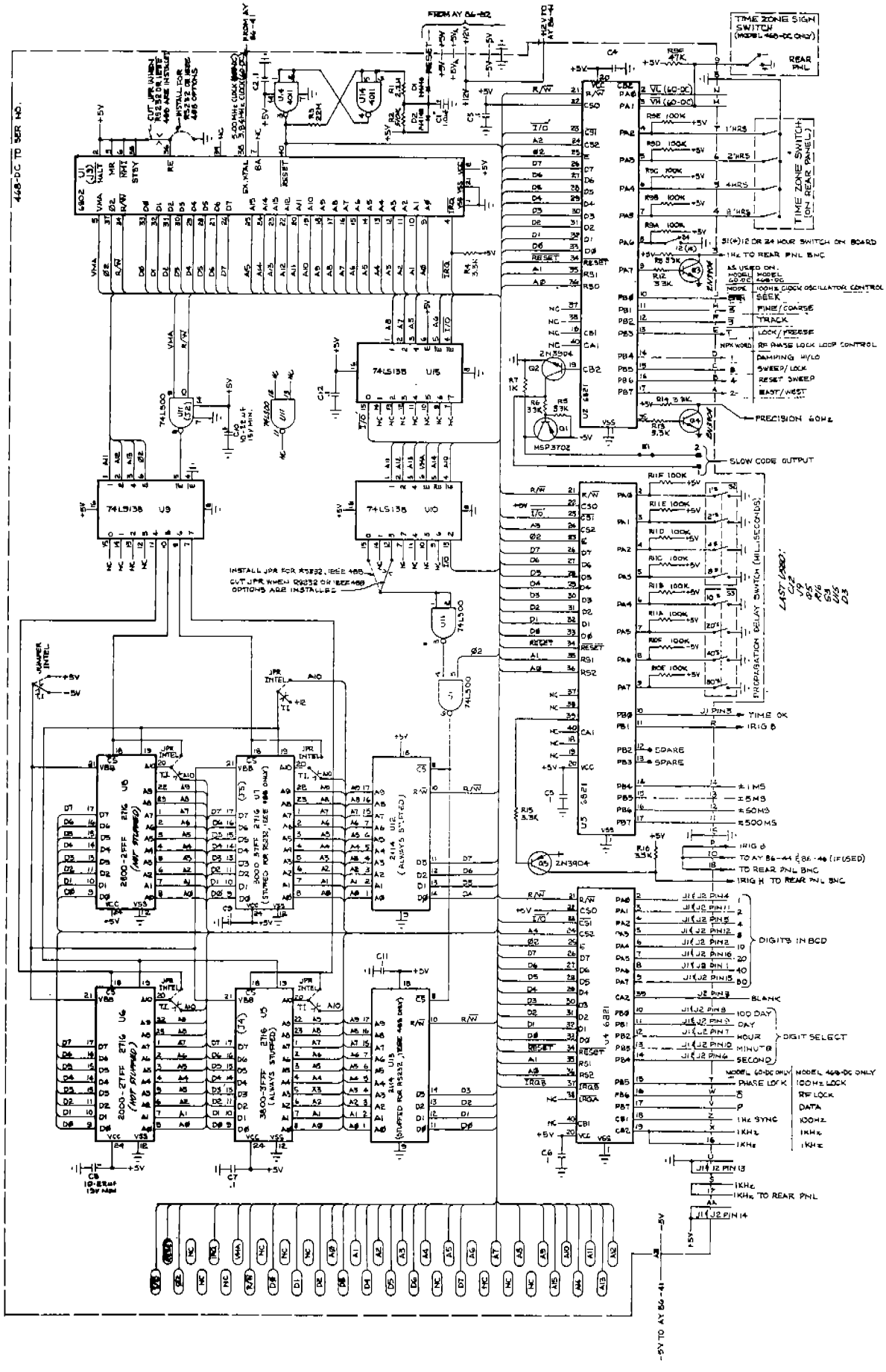
6-6 SYMBOL DESIGNATION REFERENCE 86-41 CONT

6-7 PARTS LOCATION-ASSEMBLY 86-42



6-8 SYMBOL DESIGNATION REFERENCE 86-42

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	32-29	Cap. Tant. 1.0uf 35V
C2	36-95	Cap. Monolithic .luf
C3	36-95	Cap. Monolithic .luf
C4	36-95	Cap. Monolithic .luf
C5	36-95	Cap. Monolithic .luf
C6	36-95	Cap. Monolithic .luf
C7	36-95	Cap. Monolithic .luf
C8	27-8-25*	Cap. Alum Electro 10uf 25V
C9	36-95	Cap. Monolithic .luf
C10	27-8-25*	Cap. Alum Electro 10uf 25V
C11	36-95	Cap. Monolithic .luf
C12	36-95	Cap. Monolithic .luf
	*32-45	Cap. Tant 22uf 15V may be used
D1	57-1	Diode, 1N4148
D2	57-1	Diode, 1N4148
D3	57-1	Diode, 1N4148
J1		NOT USED
J2	379-16	Socket, 16 Pin I.C.
J3	379-40	Socket, 40 Pin I.C.
J4	379-24	Socket, 24 Pin I.C.
J5	379-24	Socket, 24 Pin I.C.
J6	384-40	Connector, 40 Pin Male
J7		NOT USED
J8	318-12	Socket, 12 Pin Strip
J9	318-12	Socket, 12 Pin Strip
JPR	317-14	Jumper
Q1	175-4	Transistor, MPS3702
Q2	175-2	Transistor, 2N3904
Q3	175-2	Transistor, 2N3904
Q4	175-2	Transistor, 2N3904
Q5	175-2	Transistor, 2N3904
R1	2-153	Resistor Carbon 2.2M
R2	2-138	Resistor Carbon 510M
R3	2-177	Resistor Carbon 22M
R4	2-85	Resistor Carbon 3.3K
R5	2-85	Resistor Carbon 3.3K
R6	2-85	Resistor Carbon 3.3K
R7	2-73	Resistor Carbon 1K
R8	2-85	Resistor Carbon 3.3K
R9	11-121	Res.Carbon 100K SIP
R10	11-121	Res.Carbon 100K SIP
R11	11-121	Res.Carbon 100K SIP
R12	2-85	Resistor Carbon 3.3K
R13	2-85	Resistor Carbon 3.3K
R14	2-85	Resistor Carbon 3.3K
R15	2-85	Resistor Carbon 3.3K
R16	2-85	Resistor Carbon 3.3K
Note: All resistors are 1/4W ± 5%		
S1	65-1	Switch, 1 Pos. Dip
S2	63-2	Switch 10 Pos. Rotary
S3	63-2	Switch 10 Pos. Rotary
U1	176-6802	I.C. Motorola #MC6802
U2	176-6821	I.C. Motorola #MC6821
U3	176-6821	I.C. Motorola #MC6821
U4	176-6821	I.C. Motorola #MC6821
U5	176-2716	I.C. Intel #2716
U6		NOT USED
U7		NOT USED
U8		NOT USED
U9	176-74LS138	I.C. 74LS138
U10	176-74LS138	I.C. 74LS138
U11	176-74LS00	I.C. 74LS00
U12	176-2114	I.C. Intel #2114
U13	176-2114	I.C. Intel #2114
U14	176-4011	I.C. 4011
U15	176-74LS138	I.C. 74LS138
PWB	85-42	Printed Wiring Board


468-DC TO SER MD.
FROM AY 86-42
TIME ZONE SIGN SWITCH (MODEL 468-DC ONLY)
REAR PNL
TIME ZONE SWITCH (ON REAR PANEL)
1'HRS
2'HRS
4HRS
8'HRS
51(60)12 OR 24 HOUR SWITCH ON BOARD
1Hz TO REAR PNL BNC
AS USED ON MODEL 60-DC MODEL 468-DC
100Hz CLOCK OSCILLATOR CONTROL
SEEK
FINE/COARSE
TRACK
LOCK/RELEASE
NPK WORD
RF PHASE LOCK LOOP CONTROL
DAMPING HI/LO
SWEEP/LOCK
RESET SWEEP
EAST/WEST
PRECISION 60Hz
SLOW CODE OUTPUT
INTEGRATION DELAY SWITCH (MILLISECONDS)
J1 PIN 3 TIME OK
IRIG B
SPARE
SPARE
±1MS
±5MS
±50MS
±500MS
IRIG B
TO AY 86-44 & 86-46 (IF USED)
TO REAR PNL BNC
IRIG H TO REAR PNL BNC
DIGITS IN BCD
BLANK
100 DAY
DAY
HOUR
MINUTE
SECOND
DIGIT SELECT
MODEL 60-DC ONLY
PHASE LOCK
MODEL 468-DC ONLY
100Hz LOCK
RF LOCK
DATA
1Hz SYNC
100Hz
1KHz
1KHz
1KHz TO REAR PNL
-5V TO AY 86-41
INSTALL JPR FOR RS232, IEEE 488
CUT JPR WHEN RS232 OR IEEE 488 OPTIONS ARE INSTALLED
LAST LOAD:
C12
U9
R16
R15
R14
R13
R12
R11

6-10 SYMBOL DESIGNATION REFERENCE 86-43

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-58	Cap. Monolithic .001uf
C2	36-58	Cap. Monolithic .001uf
C3	36-58	Cap. Monolithic .001uf
C4	36-58	Cap. Monolithic .001uf
C5	36-95	Cap. Monolithic .1uf
C6	36-95	Cap. Monolithic .1uf
D1	58-4	LED, Red, H.P. #5082-4684
D2	58-4	LED, Red, H.P. #5082-4684
D3	58-4	LED, Red, H.P. #5082-4684
D4	58-4	LED, Red, H.P. #5082-4684
D5	58-4	LED, Red, H.P. #5082-4684
D6	58-4	LED, Red, H.P. #5082-4684
D7	58-1	LED, Green
D8	58-1	LED, Green
PWB	85-43	Printed Wiring Board
Q1	175-MPS A43*	Transistor MPS A43
Q2	175-2N4889	Transistor 2N4889
Q3	175-MPS A43*	Transistor MPS A43
Q4	175-2N4889	Transistor 2N4889
Q5	175-MPS A43*	Transistor MPS A43
Q6	175-2N4889	Transistor 2N4889
Q7	175-MPS A43*	Transistor MPS A43
Q8	175-2N4889	Transistor 2N4889
Q9	175-MPS A43*	Transistor MPS A43
Q10	175-2N4889	Transistor 2N4889
Q11	175-2	Transistor 2N3904
Q12	175-2	Transistor 2N3904
Q13	175-2	Transistor 2N3904
Q14	175-2	Transistor 2N3904
Q15	175-2	Transistor 2N3904

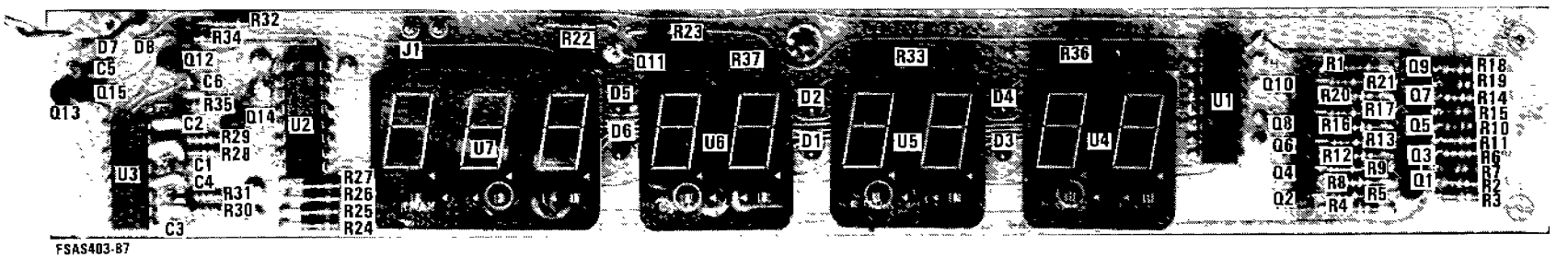
SYMBOL	TRUE TIME PART #	DESCRIPTION
R1	2-81	Res. Carbon 2.2K
R2	2-117	Res. Carbon 68K
R3	2-105	Res. Carbon 22K
R4	2-136	Res. Carbon 430K
R5	2-93	Res. Carbon 6.8K
R6	2-117	Res. Carbon 68K
R7	2-105	Res. Carbon 22K
R8	2-136	Res. Carbon 430K
R9	2-93	Res. Carbon 6.8K
R10	2-117	Res. Carbon 68K
R11	2-105	Res. Carbon 22K
R12	2-136	Res. Carbon 430K
R13	2-93	Res. Carbon 6.8K
R14	2-117	Res. Carbon 68K

* Motorola Only

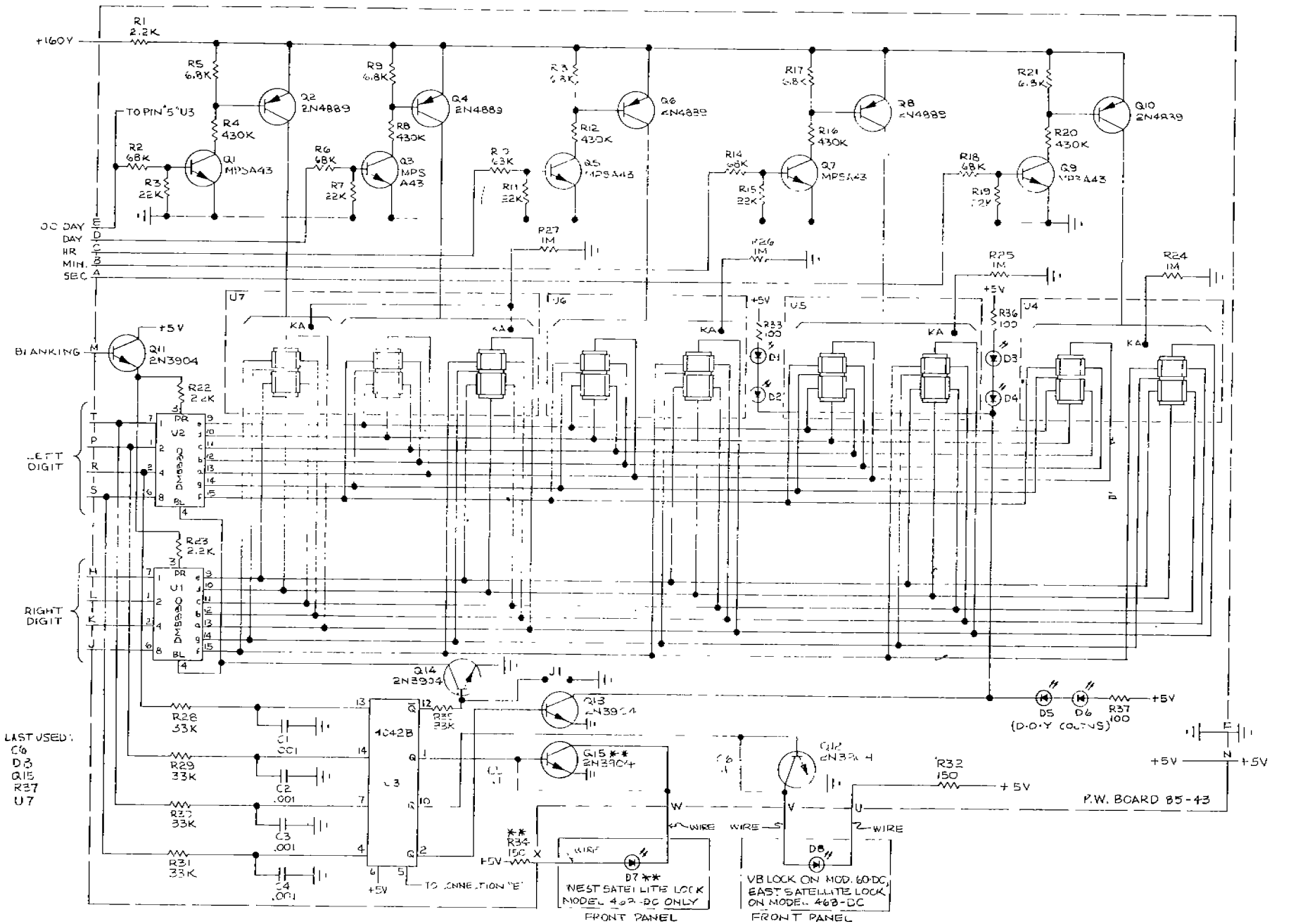
SYMBOL	TRUE TIME PART #	DESCRIPTION
R15	2-105	Res. Carbon 22K
R16	2-136	Res. Carbon 430K
R17	2-93	Res. Carbon 6.8K
R18	2-117	Res. Carbon 68K
R19	2-105	Res. Carbon 22K
R20	2-136	Res. Carbon 430K
R21	2-93	Res. Carbon 6.8K
R22	2-81	Res. Carbon 2.2K
R23	2-81	Res. Carbon 2.2K
R24	2-145	Res. Carbon 1 M
R25	2-145	Res. Carbon 1 M
R26	2-145	Res. Carbon 1 M
R27	2-145	Res. Carbon 1 M
R28	2-109	Res. Carbon 33K
R29	2-109	Res. Carbon 33K
R30	2-109	Res. Carbon 33K
R31	2-109	Res. Carbon 33K
R32	2-53	Res. Carbon 150Ω
R33	2-49	Res. Carbon 100Ω
R34	2-53	Res. Carbon 150Ω
R35	2-109	Res. Carbon 33K
R36	2-49	Res. Carbon 100Ω
R37	2-49	Res. Carbon 100Ω
U1	176-8880	I.C. National #DM8880
U2	176-8880	I.C. National #DM8880
U3	176-4042	I.C. RCA #4042B
U4	189-1	Digit Display, Beckman SP352
U5	189-1	Digit Display, Beckman SP352
U6	189-1	Digit Display, Beckman SP352
U7	189-2	Digit Display, Beckman SP353

Note: All resistors are 1/4W ± 5%

6-11 PART LOCATION-ASSEMBLY 86-43

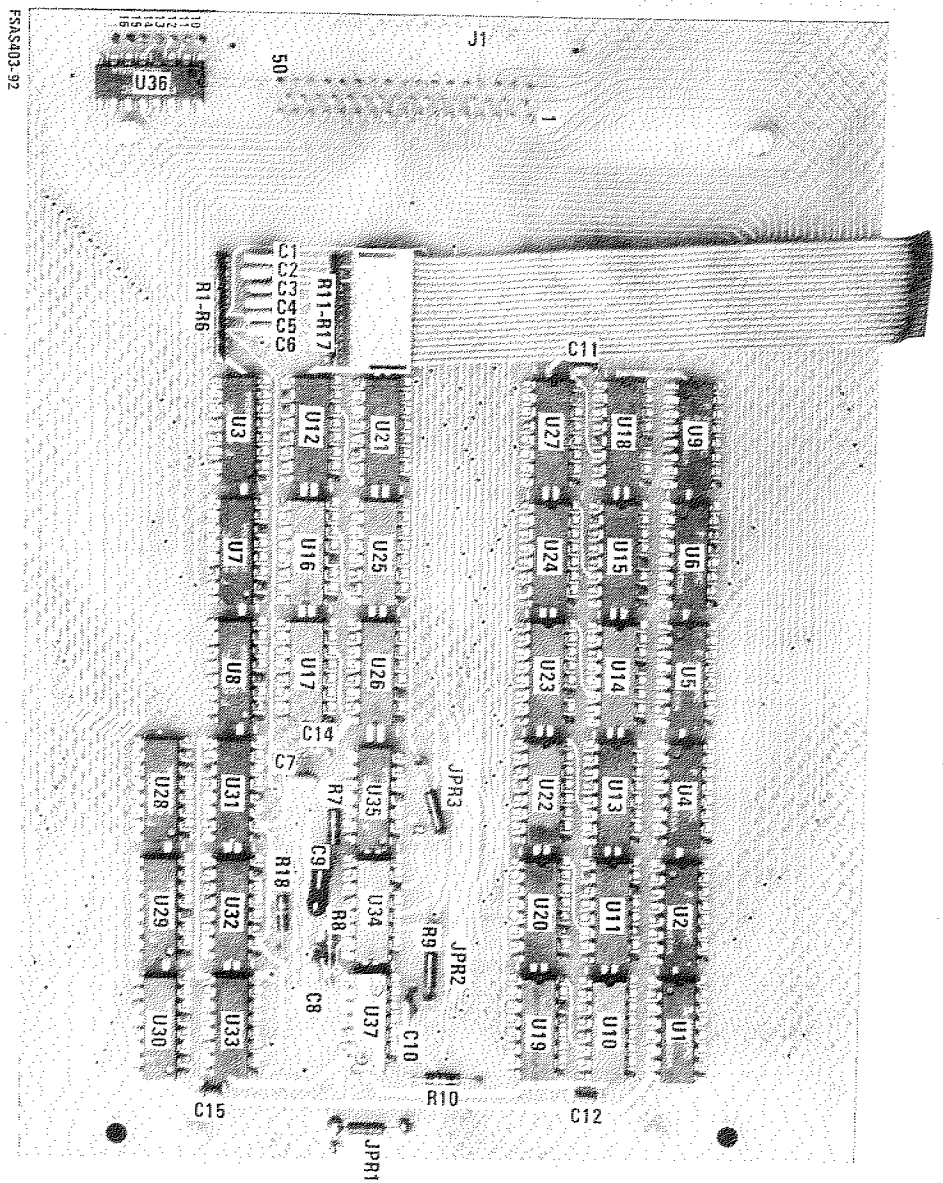


FSAS403-87



6-12 SCHEMATIC-ASSEMBLY 86-43

6-13 PARTS LOCATION-ASSEMBLY 86-44



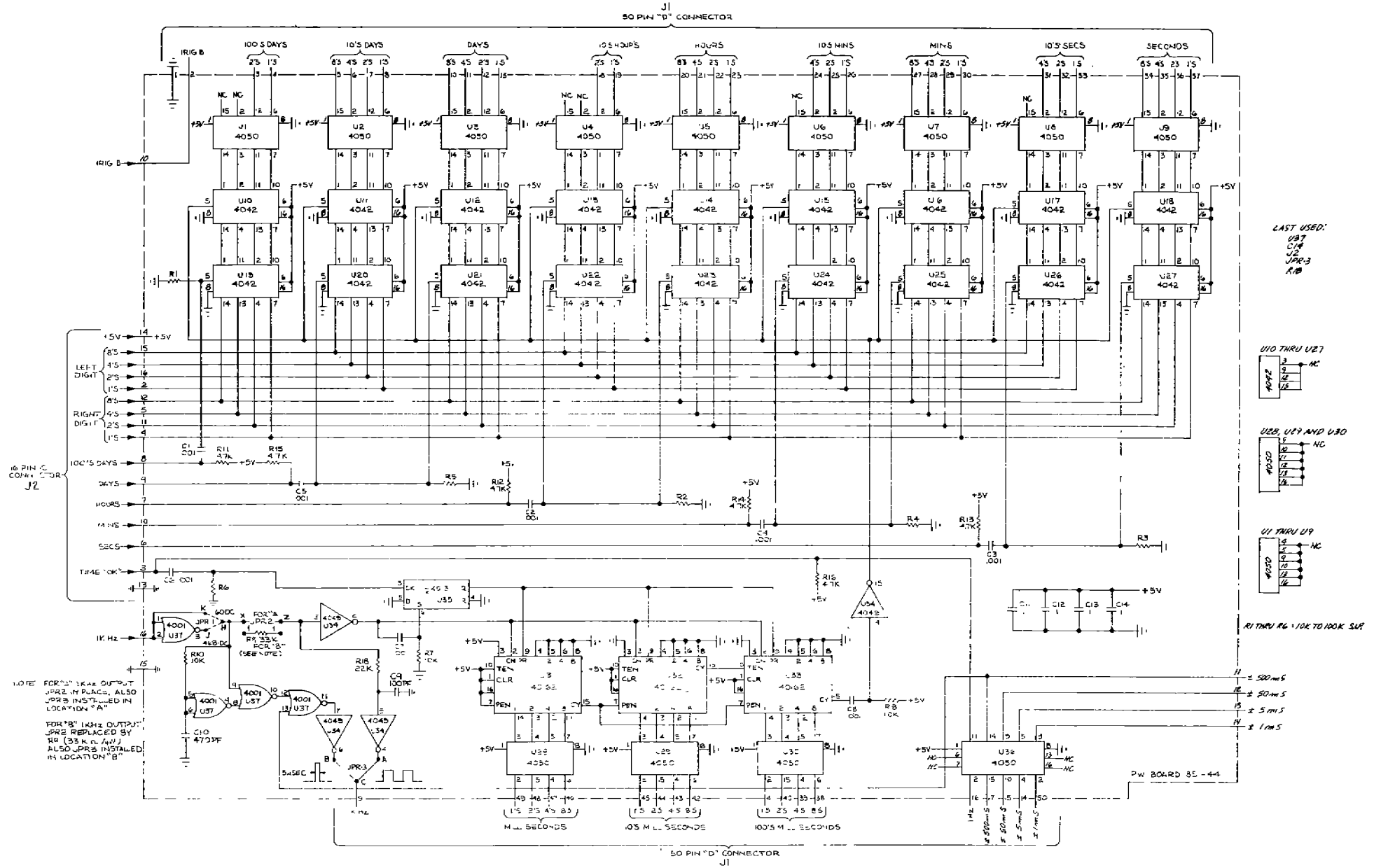
6-14 SYMBOL DESIGNATION REFERENCE 86-44

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-58	Cap. Monolithic .001uf
C2	36-58	Cap. Monolithic .001uf
C3	36-58	Cap. Monolithic .001uf
C4	36-58	Cap. Monolithic .001uf
C5	36-58	Cap. Monolithic .001uf
C6	36-58	Cap. Monolithic .001uf
C7	36-58	Cap. Monolithic .001uf
C8	36-58	Cap. Monolithic .001uf
C9	29-33	Cap. Dipped Mica 100pf
C10	36-50	Cap. Monolithic 470pf
C11	36-95	Cap. Monolithic 0.1uf
C12	36-95	Cap. Monolithic 0.1uf
C13	36-95	Cap. Monolithic 0.1uf
C14	36-95	Cap. Monolithic 0.1uf
J1	372-503	Connector 50 Pin D
J2	379-16	16 Pin I.C. Connector
JPR1	2-0	Jumper
JPR2	2-0	Jumper
JPR3	2-0	Jumper
PWB	85-44	Printed Wiring Board
R1-R6	11-121	Res. S.I. Package 100K
R7	2-97	Res. Carbon 10K
R8	2-97	Res. Carbon 10K
R9	2-109*	Res. Carbon 33K
R10	2-97	Res. Carbon 10K
R11-R17	11-89	Res. S.I.P. 4.7K
R18	2-105	Res. Carbon 22K

Note: All resistors are 1/4W + 5%

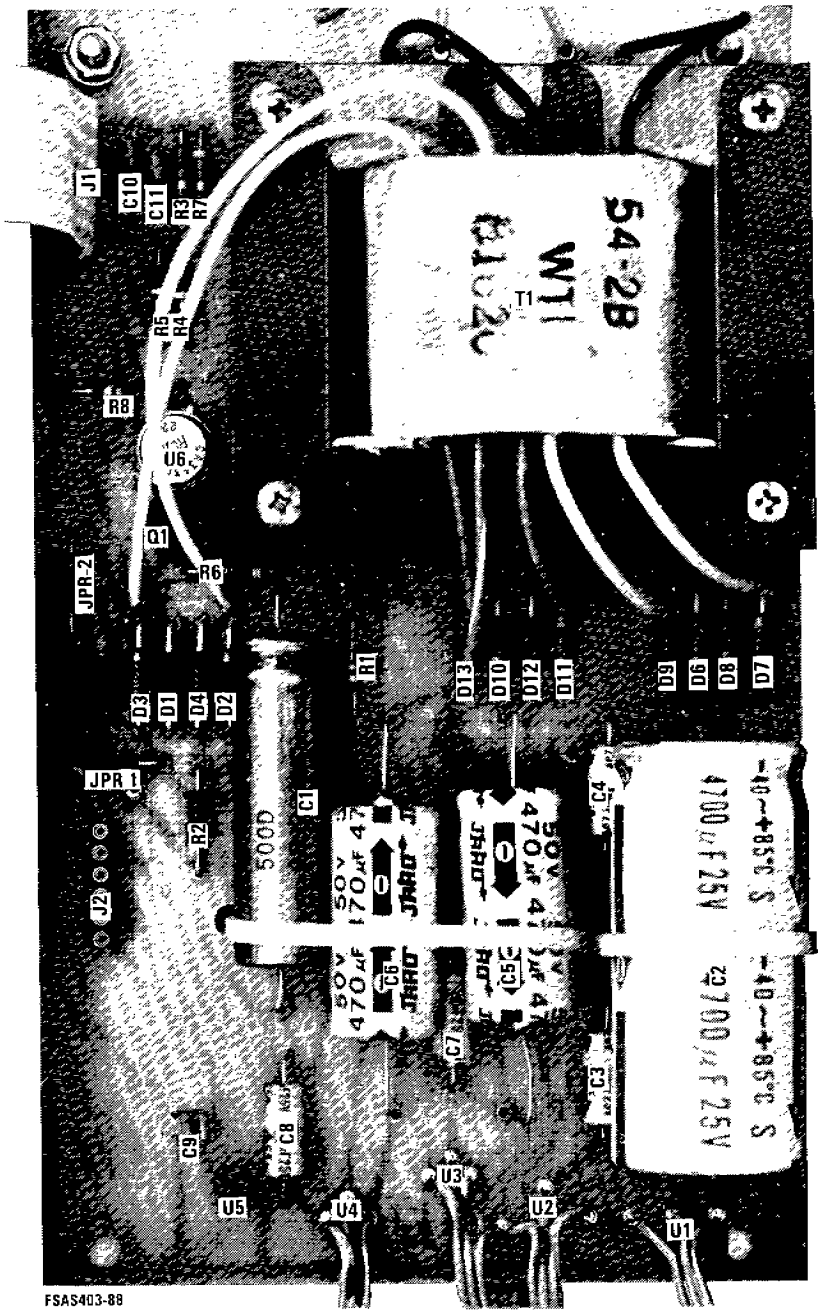
*Option replacing JPR-2 (Special Order Only)

U1	176-4050	I.C. RCA #4050
U2	176-4050	I.C. RCA #4050
U3	176-4050	I.C. RCA #4050
U4	176-4050	I.C. RCA #4050
U5	176-4050	I.C. RCA #4050
U6	176-4050	I.C. RCA #4050
U7	176-4050	I.C. RCA #4050
U8	176-4050	I.C. RCA #4050
U9	176-4050	I.C. RCA #4050
U10	176-4042	I.C. RCA #4042
U11	176-4042	I.C. RCA #4042
U12	176-4042	I.C. RCA #4042
U13	176-4042	I.C. RCA #4042
U14	176-4042	I.C. RCA #4042
U15	176-4042	I.C. RCA #4042
U16	176-4042	I.C. RCA #4042
U17	176-4042	I.C. RCA #4042
U18	176-4042	I.C. RCA #4042
U19	176-4042	I.C. RCA #4042
U20	176-4042	I.C. RCA #4042
U21	176-4042	I.C. RCA #4042
U22	176-4042	I.C. RCA #4042
U23	176-4042	I.C. RCA #4042
U24	176-4042	I.C. RCA #4042
U25	176-4042	I.C. RCA #4042
U26	176-4042	I.C. RCA #4042
U27	176-4042	I.C. RCA #4042
U28	176-4050	I.C. RCA #4050
U29	176-4050	I.C. RCA #4050
U30	176-4050	I.C. RCA #4050
U31	176-40162	I.C. RCA #40162
U32	176-40162	I.C. RCA #40162
U33	176-40162	I.C. RCA #40162
U34	176-4049	I.C. RCA #4049
U35	176-4013	I.C. RCA #4013
U36	176-4050	I.C. RCA #4050
U 37	176-4001	I.C. RCA #4001



6-15 SCHEMATIC-ASSEMBLY 86-44

6-16 PARTS LOCATION-ASSEMBLY 86-52

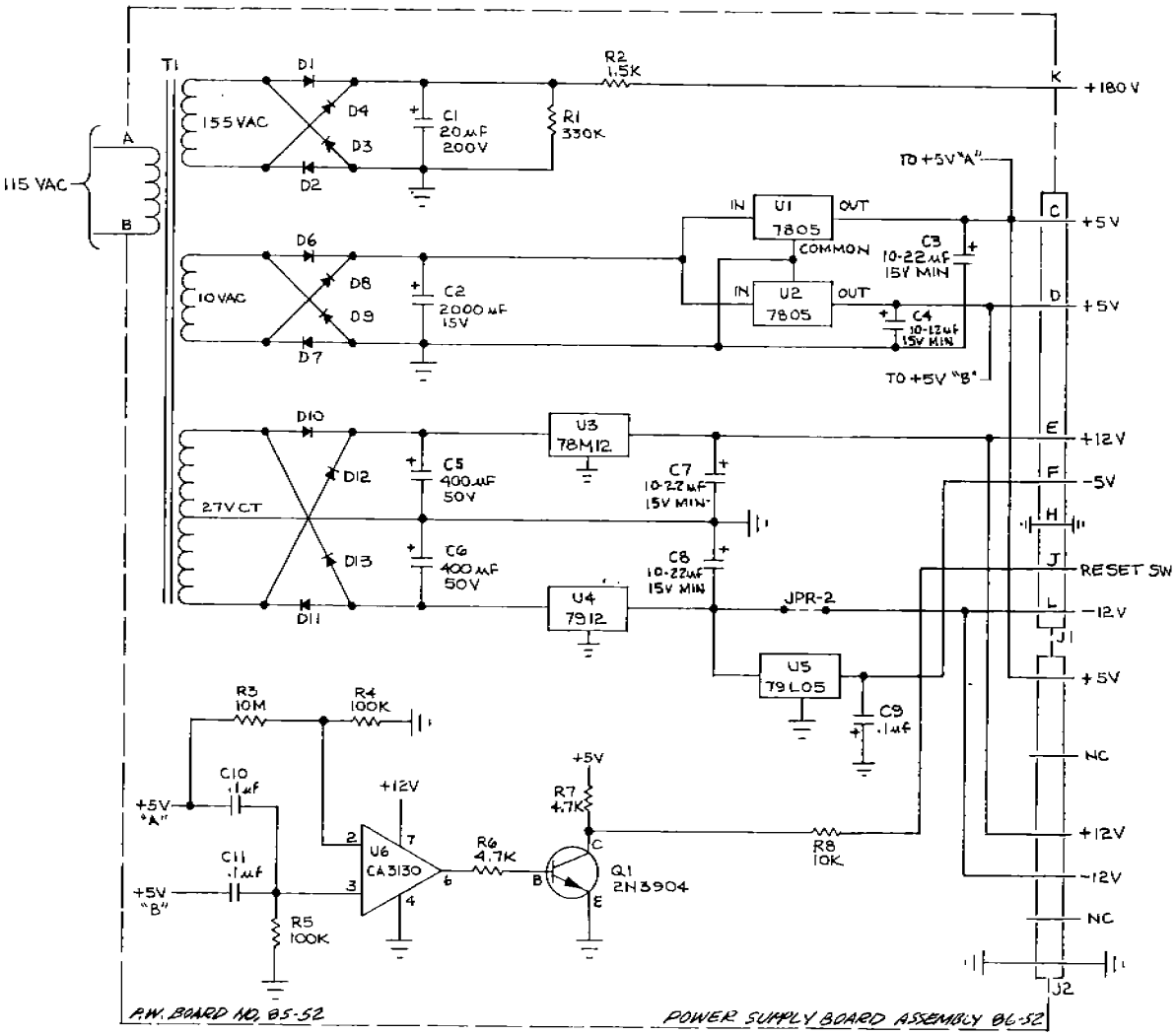


6-17 SYMBOL DESIGNATION REFERENCE 86-52

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	27-12	Cap. Electro 20uf 200V
C2	28-77	Cap. Electro 2000 uf 15V
C3	27-8-25*	Cap. Alum Electro, 10uf 25V
C4	27-8-25*	Cap. Alum Electro, 10uf 25V
C5	27-28	Cap. Electro 400uf 50V
C6	27-28	Cap. Electro 400uf 50V
C7	27-8-25*	Cap. Alum Electro, 10uf 25V
C8	27-8-25*	Cap. Alum Electro, 10uf 25V
C9	36-95	Cap. Monolithic .luf
C10	36-95	Cap. Monolithic .luf
C11	36-95	Cap. Monolithic .luf
D1	57-3	Diode 1N4005
D2	57-3	Diode 1N4005
D3	57-3	Diode 1N4005
D4	57-3	Diode 1N4005
D5		NOT USED
D6	57-2	Diode 1N4002
D7	57-2	Diode 1N4002
D8	57-2	Diode 1N4002
D9	57-2	Diode 1N4002
D10	57-2	Diode 1N4002
D11	57-2	Diode 1N4002
D12	57-2	Diode 1N4002
D13	57-2	Diode 1N4002
J1	318-7	Socket, 7 Pin Strip
J2	318-6	Socket, 6 Pin Strip
JPR-1	2-0	Jumper
JPR-2	2-0	Jumper
PWB	85-52	Printed Wiring Board
Q1	175-2	Transistors 2N3904
R1	2-133	Resistor Carbon 330K
R2	2-77	Resistor Carbon 1.5K
R3	2-169	Resistor Carbon 10MEG
R4	2-121	Resistor Carbon 100K
R5	2-121	Resistor Carbon 100K
R6	2-89	Resistor Carbon 4.7K
R7	2-89	Resistor Carbon 4.7K
R8	2-97	Resistor Carbon 10K
T1	54-2	Transformer
U1	176-7805	I.C. +5V Reg. FSC 7805UC
U2	176-7805	I.C. +5V Reg. FSC 7805UC
U3	176-78M12	I.C. +12V Reg. FSC 78M12
U4	176-7912UC	I.C. -12V Reg. FSC 7912UC
U5	176-79L05	I.C. 79L05
U6	176-3130	I.C. RCA #CA3130

* Cap. Tant 22uf 15V, Part #32-45 may be used

Note: All resistors are 1/4W ± 5%



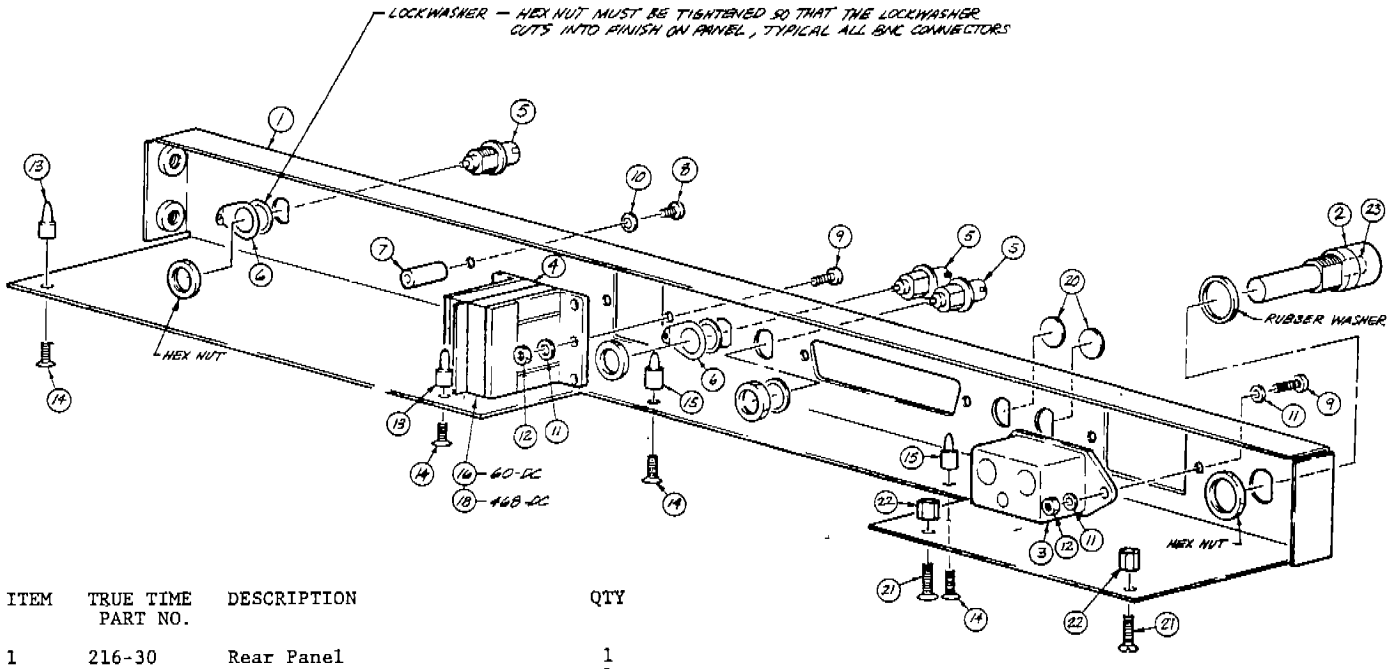
NOTE: DIODES D1 THRU D4 = IN4005
DIODES D6 THRU D13 = IN4002

NOT USED:
D5

LAST USED:
D13
R8
C11
Q1
U6
T1
JPR-2
J2

1. THIS SCHEMATIC IS TO BE USED WITH P.W. BOARD NO. 85-52 REVISION H AND SUBSEQUENT.
NOTE: UNLESS OTHERWISE SPECIFIED

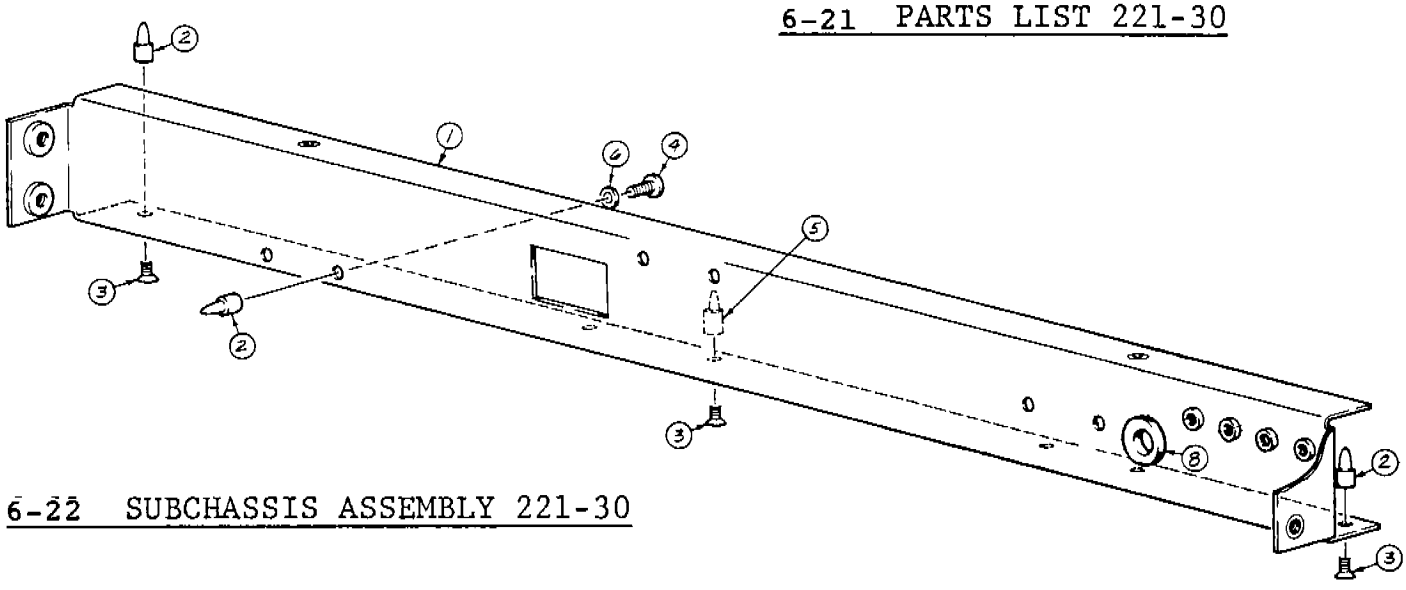
6-18 SCHEMATIC-ASSEMBLY 86-52



ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	216-30	Rear Panel	1
2	365-1	Fuse Holder	1
3	342-1	Power Socket and Line Filter	1
4	61-1	Thumb Wheel Switch	1
5	375-1	BNC Connector	3
6	256-.375	Solder Lug, .375" I.D.	2
7	255-4-4	Spacer, 4-40 x ¼" Threaded	1
8	240-4-2	Screw, 4-40 x ¼" Long PHMS	1
9	240-4-3	Screw, 4-40 x 3/8" Long PHMS	4
10	253-4	Washer #4 Flat	1.
11	265-4	Lockwasher #4 Internal	6
12	252-4	Nut 4-40 Hex	4
13	277-2	Spacer, Circuit Board, ¼" Lg	2
14	241-6-2	Screw, 6-32 x ¼" Long PHMS	4
15	277-6	Spacer, Circuit Board 3/8" lg	2
16		NOT USED	
17		NOT USED	
18	61-2	Thumb Wheel (+ and -)	1
19	134-24	Wiring Harness (not shown)	1
20	274-1	Plug, Hole	A/R
21	241-6-5	Screw, 6-32 x 5/8" Long FHMS	2
22	255-6-2	Spacer, 6-32 x ¼" Long Alum	2
23	363-.750	Fuse, 3 AG , 3/4A	1

6-19 REAR PANEL ASSEMBLY 220-30

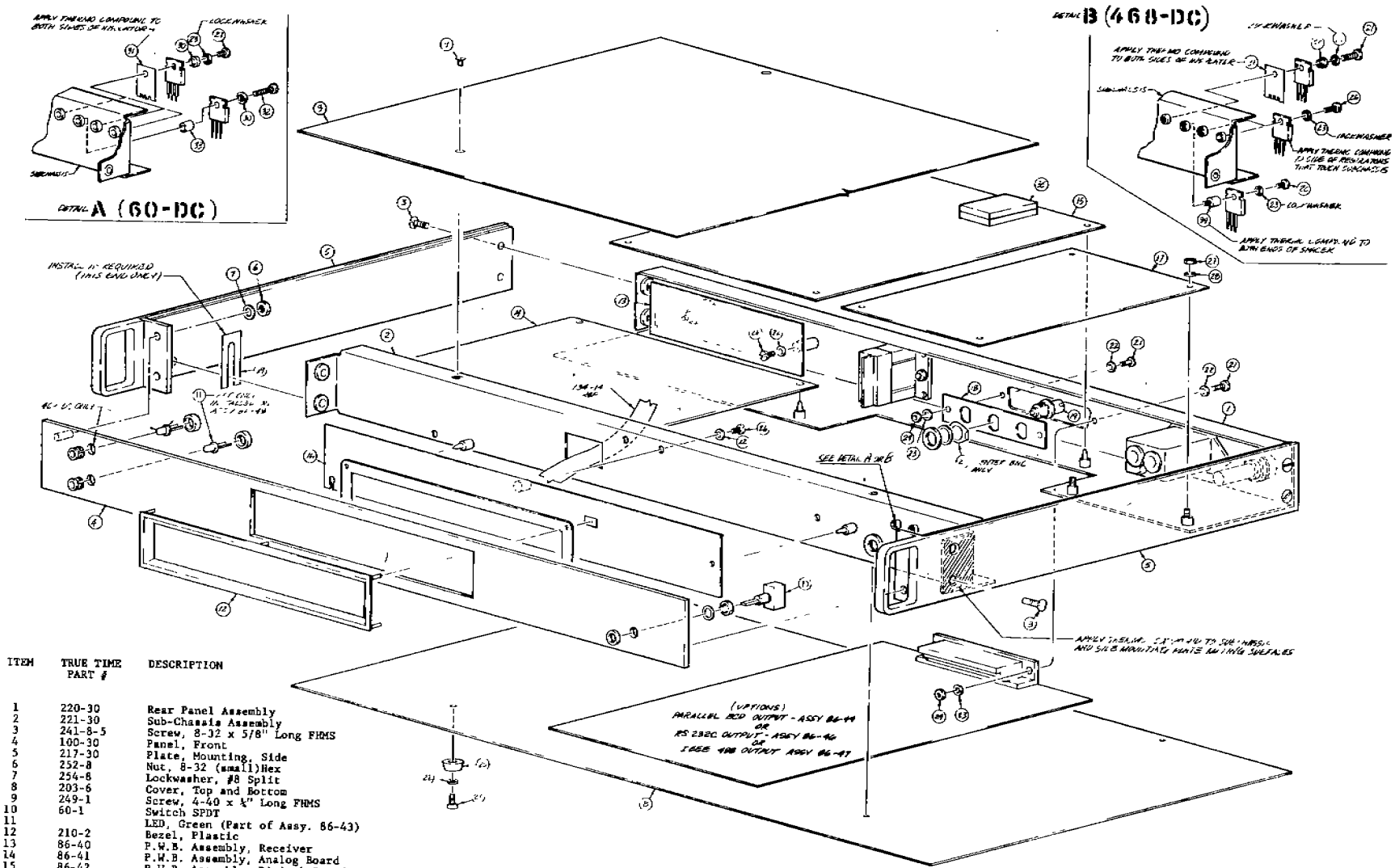
6-20 PARTS LIST 220-30



ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	215-30	Sub-Chassis	1
2	277-2	Spacer, P.W. Board ¼" Long	6
3	241-6-2	Screw, 6-32 x ¼" Long FHMS	6
4	240-6-2	Screw, 6-32 x ¼" Long PHMS	2
5	277-6	Spacer, P.W. Board, 3/8" Lg.	2
6	253-6	Washer, #6 Flat	2
7	282-1	Adhesive,Locktite	A/R
8	73-18	Grommet, Rubber	1

6-21 PARTS LIST 221-30

6-22 SUBCHASSIS ASSEMBLY 221-30



6-23 MODEL 60-DC FINAL ASSEMBLY 151-30

ITEM	TRUE TIME PART #	DESCRIPTION
1	220-30	Rear Panel Assembly
2	221-30	Sub-Chassis Assembly
3	241-8-5	Screw, 8-32 x 5/8" Long PHMS
4	100-30	Panel, Front
5	217-30	Plate, Mounting, Side
6	252-8	Nut, 8-32 (small)Hex
7	254-8	Lockwasher, #8 Split
8	203-6	Cover, Top and Bottom
9	249-1	Screw, 4-40 x ¼" Long PHMS
10	60-1	Switch SPDT
11		LED, Green (Part of Assy. 86-43)
12	210-2	Bezel, Plastic
13	86-40	P.W.B. Assembly, Receiver
14	86-41	P.W.B. Assembly, Analog Board
15	86-42	P.W.B. Assembly, Digital Board
16	86-43	P.W.B. Assembly, Display Board
17	86-52	P.W.B. Assembly, Power Supply
18	206-30	Plate - BNC Mounting
19	375-1	BNC Connector
20	256-.375	Solder Lug, .375" I.D.
21	240-4-3	Screw, 4-40 x 3/8" Long PHMS
22	253-4	Washer, #4 Flat
23	265-4	Lockwasher, #4 Internal
24	252-4	Nut, 4-40 Hex
25	261-1	Feet, Rubber
26	240-4-2	Screw, 4-40 x ¼" Long PHMS
27	252-6	Nut, 6-32 Hex
28	265-6	Lockwasher, #6 Internal
29	263-1	Shim, Chassis
30	271-4	Washer, Shoulder
31	272-2	Insulator, MICA
32	240-4-4	Screw, 4-40 x ½" Long PHMS
33	270-4-4	Spacer, #4 x ½" Long, Nylon
34		NOT USED
35	176-2716	I.C. Intel #2716
36	249-1	Screw, 4-40 x ¼" Long PHMS
37	332-2	Power Cord
38	206-1	Bracket, Rack Mounting
39	400-1	NamePlate, Product I.D.

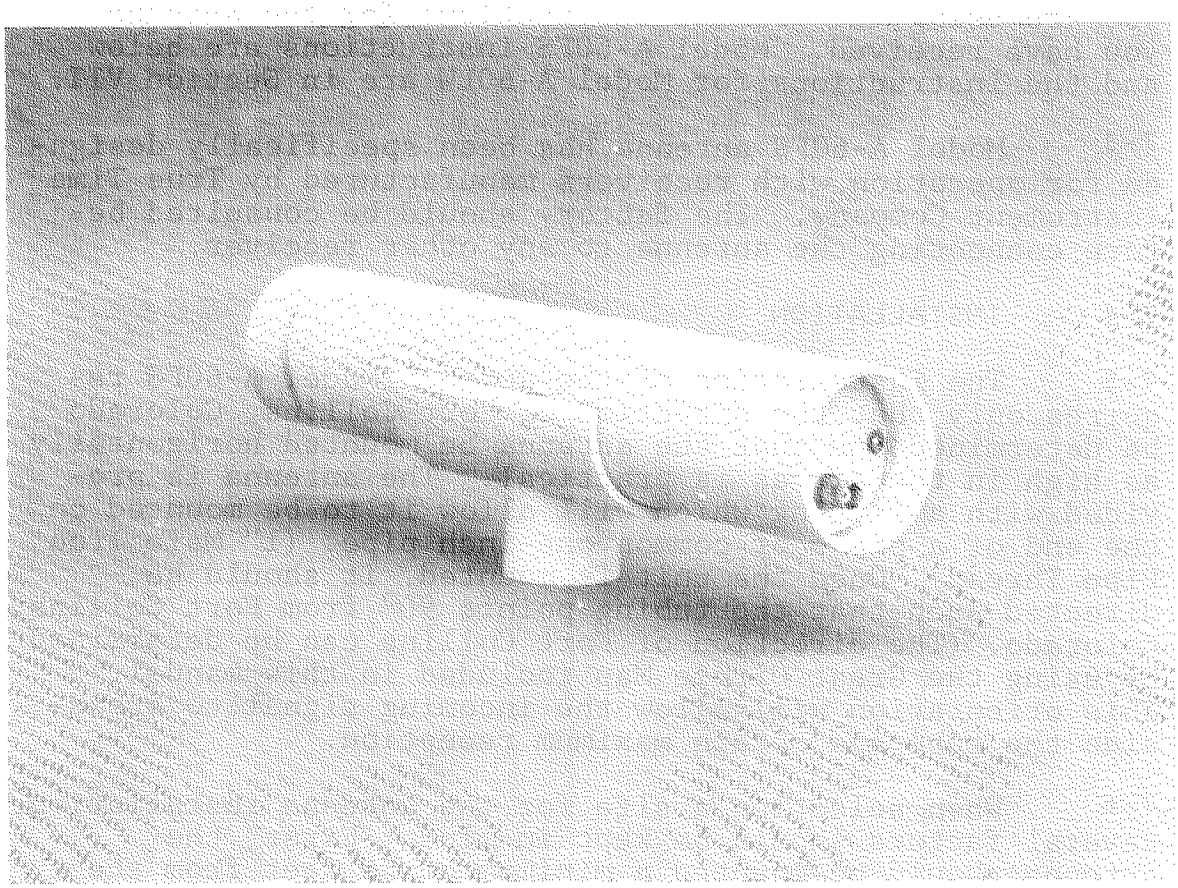
6-24 PARTS LIST 151-30

SECTION VII

ANTENNA INSTALLATION

AND SERVICE MANUAL

MODEL A-60FS



SECTION VII

ANTENNA INSTALLATION AND SERVICE MANUAL

MODEL A-60FS

7-1 INTRODUCTION

7-2 The Model A-60FS antenna is normally used in areas where the signal strength of WWVB is 100 μv/m or above. It is often used in applications which require it to be portable due to frequent moving of an installation. The first step in installing your antenna is to check the nameplate on the unit and the model number to be certain you are using the correct instructions for the antenna you have received. Model A-60FS instructions are below and the instructions for Model A-60LW are in Section VII.

7-3 Model A-60FS antenna has been specifically designed for operation with receivers manufactured by True Time Instrument Company. The factory should be consulted before connecting the antenna to any other receiver.

7-4 INSTALLATION

7-5 The installation of the antenna Model A-60FS requires only that the direction of Fort Collins, Colorado be determined and that the antenna be mounted horizontally as high in the air as is practical. The antenna is provided with a fitting which will allow it to be mounted on the end of a piece of common one-inch pipe. (1" Male Iron Pipe Thread) Once the unit is mounted, it should be directed such that the tubing points 90° from Fort Collins, Colorado. (The direction of Fort Collins can be determined by using the Great Circle Map included in this manual.) This orientation will allow the incoming signal to broadside the tube and obtain maximum reception.

7-6 When selecting a site for the antenna installation, several factors should be kept in mind. First, the antenna should be mounted a minimum of 25 feet from the receiver to prevent regeneration. Second, the antenna should not be mounted close to any steel structures (roof decking, pipes, air conditioning, etc.). Third, the signal-to-noise ratio will be improved by locating the antenna as far as practical from any local R.F. noise source (large electric motors, power lines, etc.). Finally,

in most cases the antenna will not be able to receive signal from WWVB is installed inside of a building, it must be outside.

7-7 After the unit is mounted, attach the lead-in coax (RG-58/U recommended) to the output BNC and the installation is complete. The antenna has been provided with a trimmer capacitor which has been factory tuned and locked for maximum reception. This antenna should not need retuning except in cases of extreme temperature, or after a long period of aging. Tuning procedure is included in the Maintenance Section of this manual.

7-8 MAINTENANCE

7-9 The Model A-60FS antenna contains a ferrite rod antenna coil and a preamp/line driver. The preamp contains only three active devices and should not require maintenance under normal conditions.

7-10 The antenna may need re-tuning when operating in extreme temperatures. Then it will be evident that the resonate frequency has shifted from the factory set 60 kHz, and this will cause a loss in signal strength. The best method of re-tuning the antenna is depicted in the block diagram below.

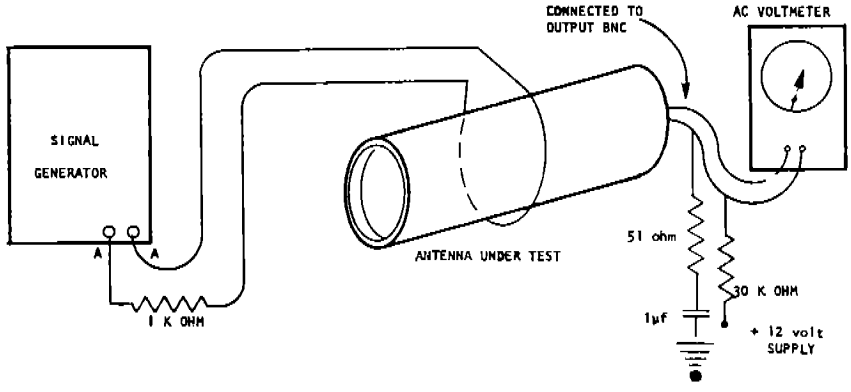


FIGURE 7-1 A60FS Block Diagram

7-11 Apply 12 volts through a 30K ohm resistor to the BNC connector, and couple in a 60.0 kHz signal by wrapping a single turn of wire around the center of the antenna. Connect the wire to the signal generator through a 1K ohm resistor; this resistor provides a constant current source.

7-12 This set-up and tuning should be performed at the approximate temperature the antenna is intended to operate. After the equipment is set-up as shown, remove the slot-head screw in the end of the antenna to allow access to the internal trimmer. The internal ceramic trimmer is adjusted with a small slot screwdriver. Tune the trimmer for maximum output at the BNC connector. Reinstall the screw. The antenna is now re-tuned for 60 kHz resonance at the temperature at which the tuning has been performed.

7-13 TROUBLESHOOTING

7-14 As mentioned in the Maintenance Section, the antenna contains only three active devices, all bipolar transistors. The most common types of failure that might be expected are:

a. Antenna has become de-tuned due to temperature extremes or aging.
b. Ferrite rod broken due to mechanical shock.
c. Failure of one of the devices.

7-15 The first step in determining the cause of antenna failure is to set-up the test equipment as shown in the block diagram in the Section above. With a 80mv (P-P) at generator output measured at Point AA, the antenna output should measure about 3.5mv at resonance on the A.C. Voltmeter (10mv P-P). If this level is not present, re-tune the trimmer to peak output. Once the resonance is set with the trimmer, the -3 db points should occur at $\pm$500 Hz from resonance.

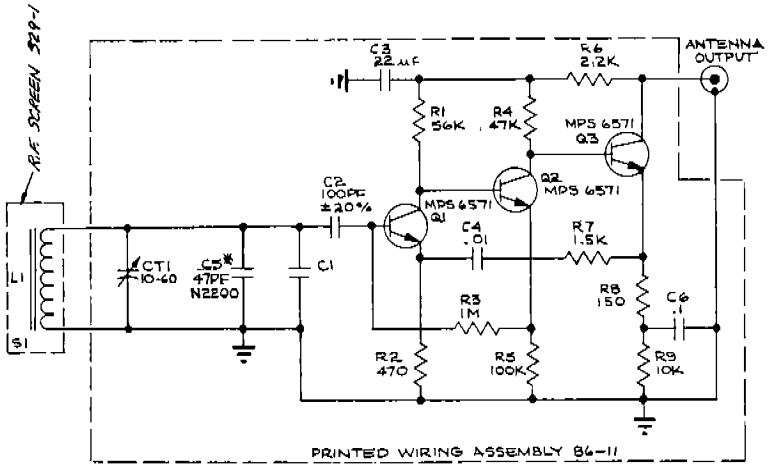
NOTE: Resonance frequency and Q will be shifted by nearby conductors; attempt to keep large conductors a minimum of 2 feet away from the antenna when in use or during test.

7-16 A broken ferrite rod will first become evident due to the inability to tune and obtain the proper output. To check for a broken rod, slowly increase the frequency of the generator and if the antenna resonance is found above 61 kHz, the cause is most likely a broken ferrite rod.

7-17 After re-tuning, if the antenna does not have an output, as above, it should be returned to the factory for repair.

7-18 In some cases it may not be practical to return the antenna. Below is information for performing field repairs.

7-19 After it has been determined by the above tests that the antenna is defective, use a sharp knife and cut open the end plate on the tubing on which the output connector is mounted. The preamp assembly can then be pulled out and repaired with the data and schematic on the following page. After repairs are complete, the end can be resealed with common PVC cement.



SYMBOL	DESCRIPTION	PART #	QTY
C1	Cap. Ceramic Disc. 150pf	26-18A	1
C2	Cap. Monolithic 100pf ±20%	36-33	1
C3	Cap. Tantalum 22uf	32-45	1
C4	Cap. Monolithic .01uf	36-83	1
C5	Cap. Dipped Mica 47pf	29-24	1
C6	Cap. Monolithic .1uf	36-95	1
Q1	Transistor MPS 6571	175-5	3
Q2	Transistor MPS 6571	175-5	3
Q3	Transistor MPS 6571	175-5	3
R1	Resistor Carbon 56K	2-115	1
R2	Resistor Carbon 470	2-65	1
R3	Resistor Carbon 1M	2-145	1
R4	Resistor Carbon 47K	2-113	1
R5	Resistor Carbon 100K	2-121	1
R6	Resistor Carbon 2.2K	2-81	1
R7	Resistor Carbon 1.5K	2-77	1
R8	Resistor Carbon 150	2-53	1
R9	Resistor Carbon 10K	2-97	1
CT1	Cap, Variable 10-60pf	33-60	1
PWB	Printed Wiring Board, Antenna Preamp	85-11	1
	NOTE: FOR A-77.5FS ONLY		
C5	Omit		
C1	Cap. Dipped Mica 68pf	29-29	1

FIGURE 7-2

SECTION VIII

WWVB TIME CODE

8-1 INTRODUCTION

8-2 The National Bureau of Standards radio station WWVB, located in Fort Collins, Colorado (Latitude 40° 41' 28.3"N, Longitude 105° 02' 39.5"W), transmits a modified IRIG H time code with a power of 13 KW E.R.P.. The modified IRIG H time code is a binary coded decimal (BCD) with a one-minute time frame.

8-3 CODE AND CARRIER

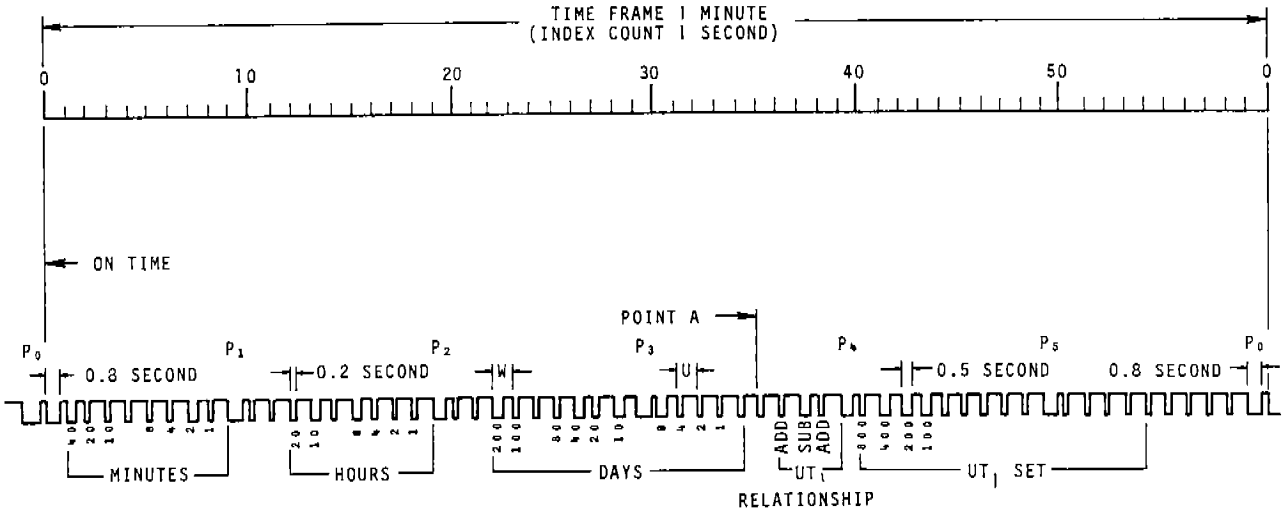
8-4 On July 1, 1965, WWVB began broadcasting time information using a level-shift carrier time code. The code is broadcast continuously and is synchronized with the 60 kHz carrier signal. Beginning in mid 1973 these broadcasts were made on a continuous basis eliminating the periodic Tuesday shutdown.

8-5 MARKER GENERATION

8-6 As shown in the Figure below, the signal consists of 60 markers each minute, with one marker each second. (Time progresses from left to right.) Each marker is generated by reducing the power of the carrier by 10 db at the beginning of the corresponding second and restoring it.

1. 0.2 seconds later for an uncoded marker or binary "zero".
2. 0.5 seconds later for a binary "one".
3. 0.8 seconds later for a 10-second position marker or for a minute reference marker.

Chart depicts 10 db carrier level drops as transmitted.



1 PPM FRAME REFERENCE MARKERS
BINARY CODED DECIMAL TIME-OF-YEAR CODE WORD (23 DIGITS)
CONTROL FUNCTIONS (15 DIGITS) USED FOR UT_1 CORRECTIONS
6 PPM POSITION IDENTIFIER MARKERS AND PULSES (P_0 THRU P_5)
(REDUCED CARRIER 0.8 SECOND DURATION PLUS 0.2 SECOND DURATION PULSE)
W - WEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.5 SECOND - BINARY ONE)
U - UNWEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.2 SECOND - BINARY ZERO)

TIME AT POINT A
258 DAYS
18 HOURS
42 MINUTES
34.3 SECONDS

8-7. MARKER ORDER AND GROUPS

8-8 The 10-second position markers, labeled PO through P5 on the diagram, occur respectively as the 59th, 9th, 19th, 29th, 39th, and 49th second pulses of each minute. The minute reference marker begins at zero seconds. Uncoded markers occur periodically as the 4th, 14th, 24th, 34th, 44th, 54th seconds pulses and also as the 10th, 11th, 20th, 21st, 35th, 55th, 56th, 57th, and 58th seconds pulses of each minute. Thus every minute contains twelve groups of five markers, each group ending either with a position marker or an uncoded marker.

8-9 INFORMATION SETS

8-10 Each minute the code presents time-of-year information in minutes, hours, day-of-the-year, and the actual milliseconds difference between the time as broadcast and the best known estimate of UT_1. The first two BCD groups in the minute specifies the minute of the hour; the third and fourth BCD groups make up a set which specifies the hour of the day; the fifth, sixth, and seventh groups form a set which specifies the day-of-year. A set made up of the ninth, tenth, and eleventh BCD groups, specifies the number of milliseconds to be added or subtracted from the code time as broadcast in order to obtain UT_1. The relationship of the UT_1 scale to the time as coded is indicated in the eighth group.

8-11 If UT_1 is "slow" with respect to the code time, a binary "one" labeled SUB (subtract) on the preceding Figure, will be broadcast in the eighth group during the 38th second of the minute. If UT_1 is "fast" with respect to the code time a binary "one", labeled ADD, will be broadcast in the eighth group during the 37th and 39th seconds of the minute. The twelfth group is not used to convey information.

8-12 DIGITAL INFORMATION

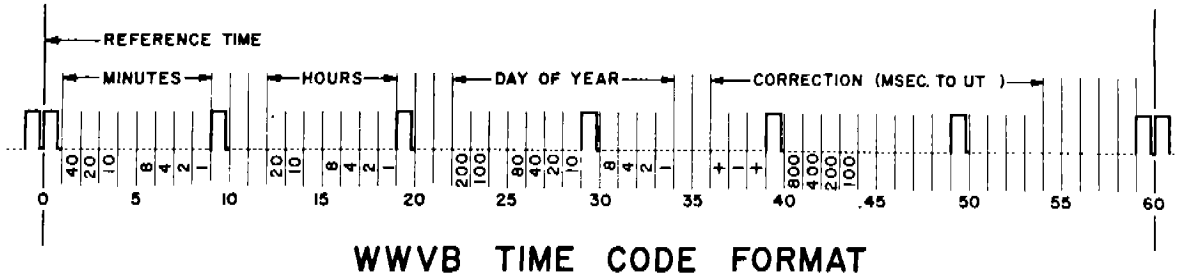
8-13 When used to convey numerical information, the four coded markers used as digits in a BCD group are indexed 8-4-2-1 in that order. Sometimes only the last two or three of the coded markers in a group are needed, as in the first groups in the minutes, hours, and days sets. In these cases, the markers are indexed 2-1, or 4-2-1, accordingly. The indices of the first group in each set which contains two groups are multiplied by 10. Those of the second group of such a set are multiplied by 1. The indices of the first group in each set which contains three groups are multiplied by 100; those of the second group are multiplied by 10, and those of the third group by 1.

8-14 Example: A specific example is indicated in the Figure 8-1. The occurrence of two binary "ones" in the "minutes set" indicates that the minute contemplated is the 40 + 2 = 42nd minute. Similarly, the two binary "ones" in the "hours set" indicate the 10 + 8 = 18th hour of the day, while the four binary "ones" in the "days set" indicate the 200 + 40 + 10 + 8 = 258th day of the year.

8-15 It is seen from the "UTI Relationship" group and the "UTI Set" that one should subtract, from any second in this minute, 400 + 200 + 100 = 700 milliseconds to get an estimate of UTI. For example, the 35th UTI interval would end 700 milliseconds (or 0.7 second) later than the end of the 35th second. In other words, the UTI scale reading for the end of the 35th second would be 18h 42m 34.3s, since 35.0s - 0.7s = 34.3s.

8-16 If more detailed and further information on these broadcasts are required please write to the address on the next page and ask for a copy of the current issue of National Bureau of Standards Publication #432.

Time and Frequency Division
Institute for Basic Standards
National Bureau of Standards
Boulder, Colorado 80303



WWVB TIME CODE FORMAT

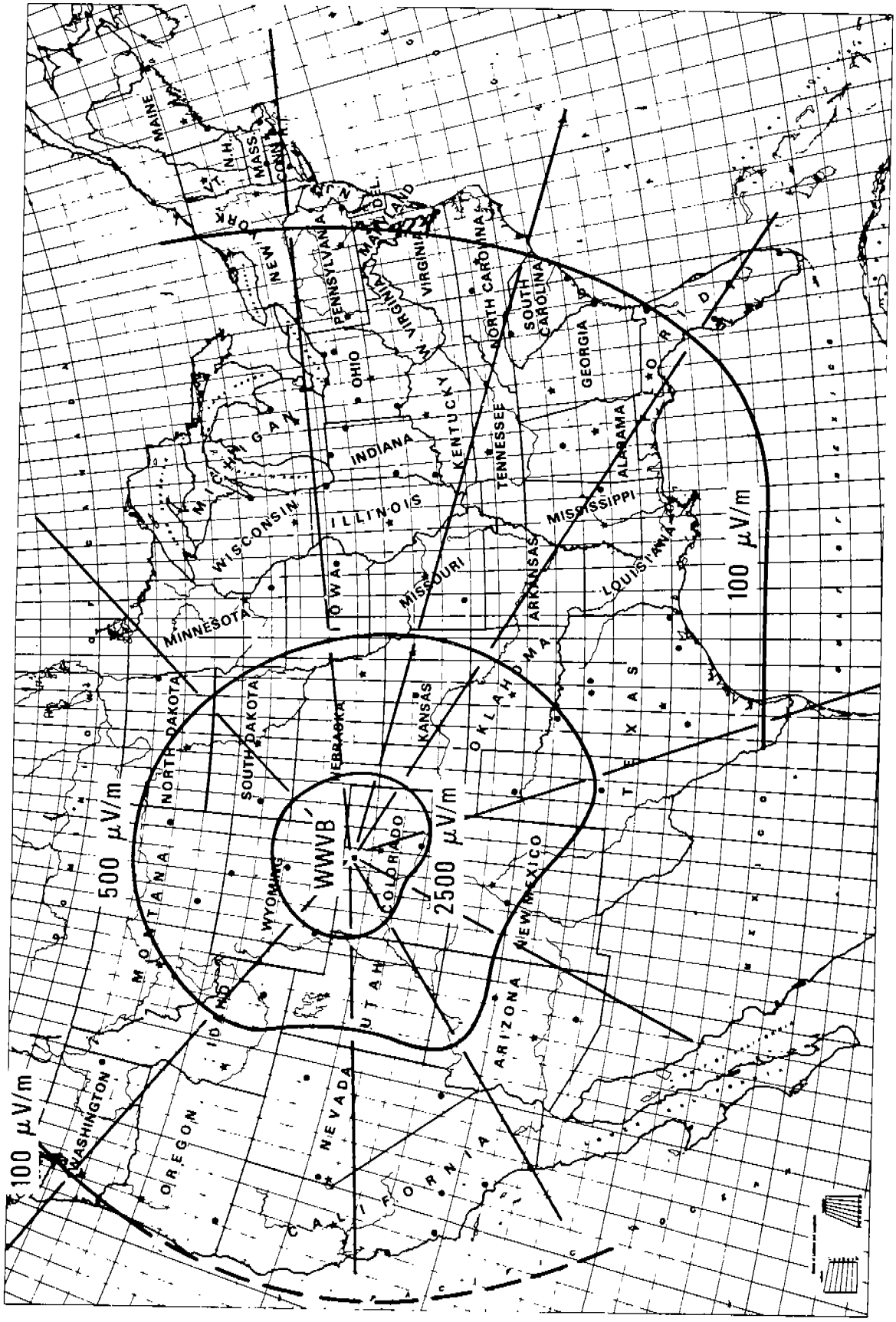
SECTION IX

GREAT CIRCLE MAP
OF THE NORTHERN PORTION OF THE
WESTERN HEMISPHERE CENTERED ON
FORT COLLINS, COLORADO

TO DETERMINE THE COMPASS HEADING FOR ANTENNA ORIENTATION FROM YOUR LOCATION TO FORT COLLINS, COLORADO: Draw a straight line from the receiving location through Fort Collins, Colorado point ⊕ on the map and continue until the line intersects the outer ring. The point at which the line intersects the outer ring indicates the compass heading for Fort Collins from you location.

SECTION X

MEASURED FIELD INTENSITY OF WWVB



SECTION XI

IRIG B AND IRIG H TIME CODE FORMAT

11-1 INTRODUCTION

11-2 The IRIG B Time Code as outputted from the Model 60-DC, and IRIG H if optionally ordered, is as described in "IRIG STANDARD TIME FORMATS" Tele-Communications Working Group, Inter-Range Instrumentation Group, Range Commanders Council, IRIG Document 104-70. This document is published by Secretariat, Range Commanders Council, White Sands Missile Range, New Mexico, 88002 dated August, 1970.

11-3 The standard time formats described in this publication were designed for use in missile, satellite and space research programs which require the use of a standardized time format for the efficient interchange of test data among the various users of the data. These formats are suitable for recording on magnetic tape, oscillographs, film and for real-time transmission in both automatic and manual data reduction. The IRIG B format from the Model 60-DC is suitable for remote display driving, recording on magnetic tape and many other uses. When the output is used as IRIG B in the strict sense as described by the above mentioned document, the output must be in Universal Coordinated Time (UTC) and not converted to 12-hour basis or local time zone as is the capability of this instrument. The same is of course true of the IRIG H output.

11-4 IRIG CODE FORMAT

11-5 The IRIG B and IRIG H Time Code as provided by the Model 60-DC is a serial time format with two coded expressions. The first expression is a time-of-year code word in Binary Coded Decimal (BCD) notation as days, hours, minutes and seconds. The second expression used here is a set of elements for encoding control functions which are used in the Model 60-DC to provide the user with worst case estimate of the timing accuracy. The estimate for this timing accurace is discussed in Sections 3-49 through 3-53 of this manual. The third expression sometimes found in the IRIG code, which is an expression of time-of-day in Straight Binary Seconds (SBS) notation, is not outputted by the Model 60-DC.

11-6 Each pulse, or element, in the format of the level-shift encoded signal has a leading edge which is "on time". The repetition rate of the elements in the IRIG B is 100 pulses per second, and 1 pulse per second in IRIG H. The index count interval, or the time between the leading edges of two consecutive elements is 0.01 seconds with IRIG B and 1 second with IRIG H.

11-7 The time frame format begins with a frame reference marker and consists of all the elements between two consecutive frame reference markers. This frame reference marker consists of a consecutive position identifier element and a "P" reference element each having a duration of 0.008 seconds in IRIG B and .8 seconds in IRIG H. The on time reference point of time frame is the leading edge of the second pulse. The repetition rate of the time frame called the "time frame rate" is 1 fps (frame per second) with IRIG B and 1 fpm (frame per minute) with IRIG H. P_0. occurs one index count interval before the frame reference point and each succeeding position identifier (P_1, P_2, P_3, P_4, etc.) occurs every succeeding tenth element. The repetition rate them, of the position identifiers is 10pps in IRIG B and 6ppm in IRIG H. There are 7 position identifiers per IRIG H frame and 11 position identifiers per IRIG B frame.

11-8 The BCD time-of-year code word is pulse width coded. A binary "1" element has a duration of 0.005 seconds, a binary "0" has a duration of 0.002 seconds for IRIG B. IRIG H in .5 seconds for a "1" and .2 seconds for a "0". This format is then used to encode the BCD time-of-year code word which consists of decimal digits in a 1-2-4-8 binary sequence.

11-9 When the IRIG B from the Model 60-DC is in the amplitude modulated 1 kHz format, the sine wave carrier frequency is synchronized to have a positive going axis crossing coincident with the leading edge of the modulating format elements. The IRIG H format is D.C. level shift format as supplied by the factory. See Section 3-44.

11-10 Figure 11-1 on the following page depicts the IRIG B Time Code, and Figure 11-2 depicts IRIG H.

11-11 CONTROL FUNCTIONS

11-12 The control functions provide the user of the IRIG B Time Code with a record in their recording of the estimated worst case accuracy of the Model 60-DC time information. This is more fully covered in Section
A "1" or .005 second pulse width in the following loca-

tions signify the accuracy specifically.

Control Function Element 6 (or time P_r+550ms) indicates ±1. 0ms worst case
Control Function Element 7 (or time P_r+560ms) indicates ±5. 0ms worst case
Control Function Element 8 (or time P_r+570ms) indicates ±50.0ms worst case
Control Function Element 9 (or time P_r+580ms) indicates ±500.0ms worst case

11-13 This information is also utilized by the True Time Model RD-B to duplicate the display of the 60-DC Master Clock. At ±50ms the colons are flashed, and at ±500ms the display will blink on the Model RD-B.

11-14 The IRIG H Time Code does not contain these control bits. These have not been included due to the relative time frames and usage of this code as opposed to the IRIG B Code.

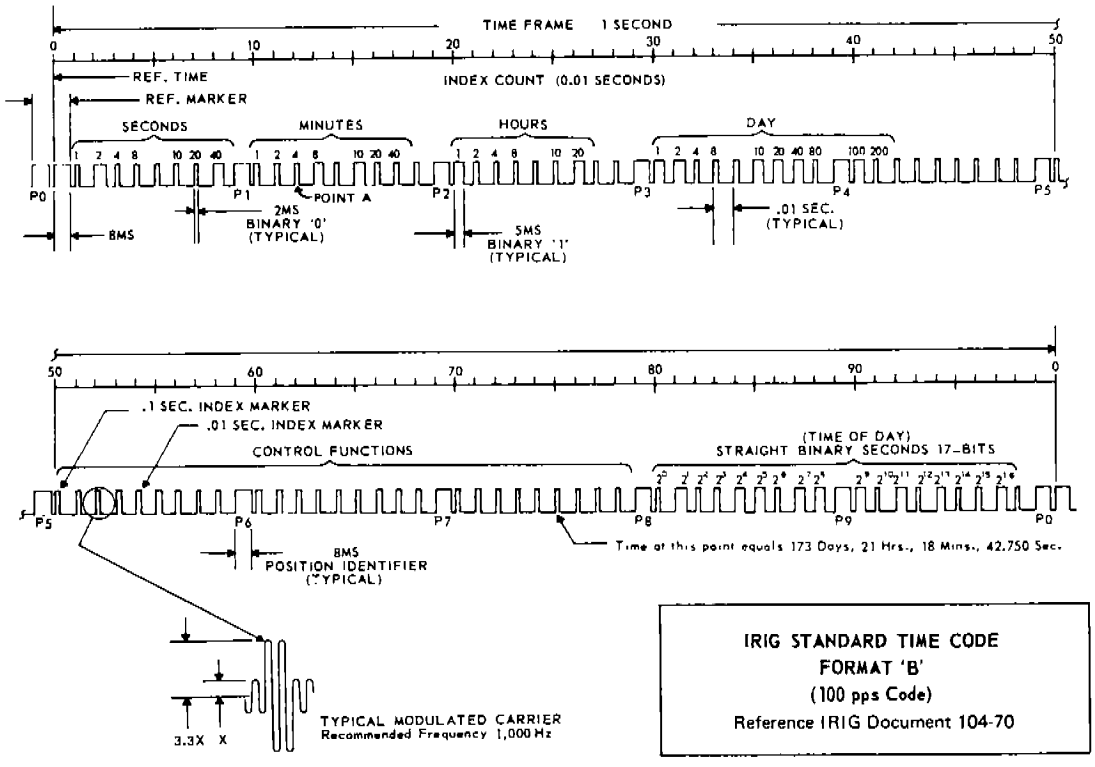


FIGURE 11-1 IRIG B TIME CODE FORMAT

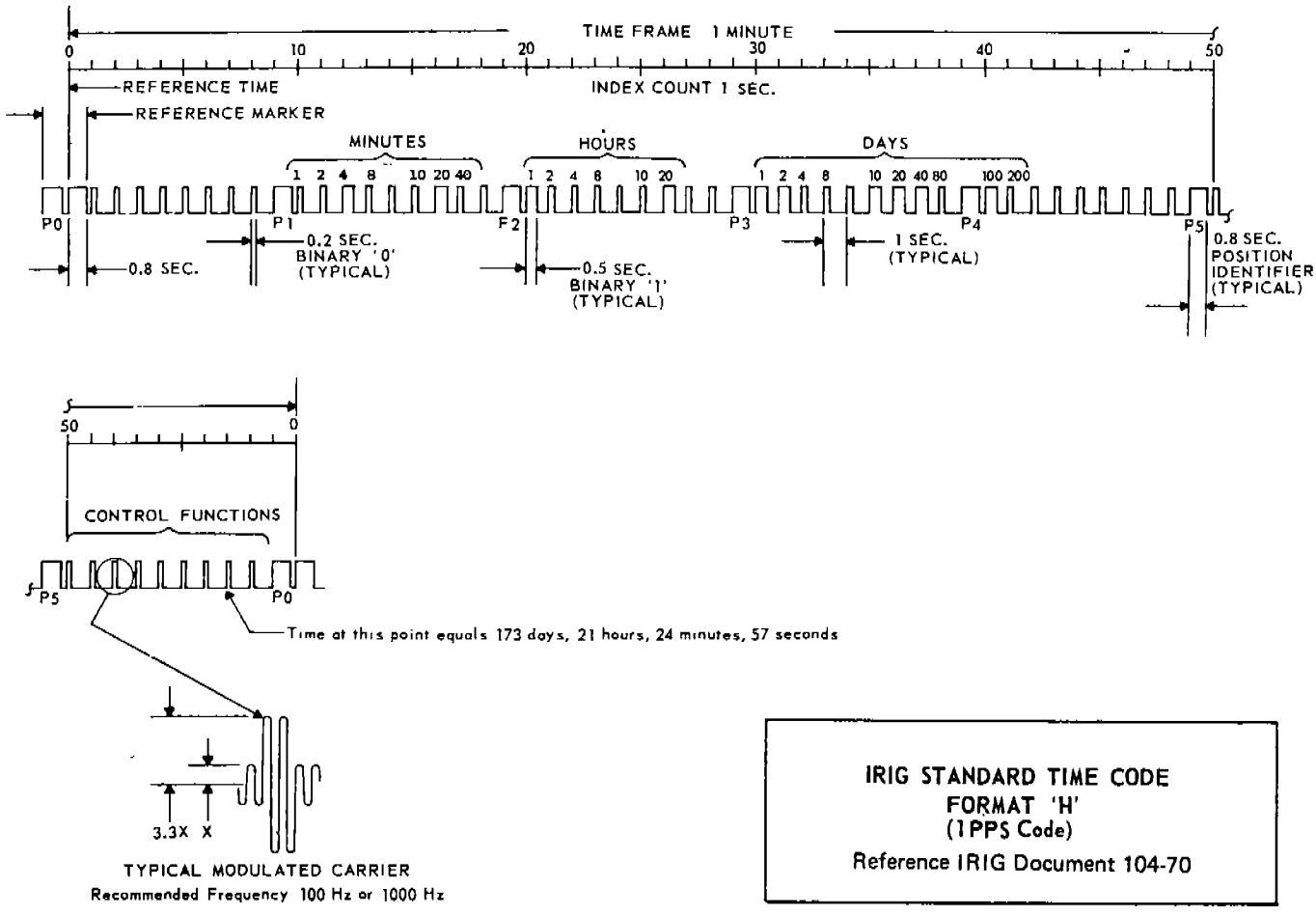


FIGURE 11-2 IRIG H TIME CODE FORMAT

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